A 140-GHz 40-mW Receiver with LO Generation and Phase Shifting for Beamforming Applications

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***Abstract*—This paper presents a 140-GHz heterodyne receiver that employs an RF path with low-impedance interfaces for stability, two PLLs for low-power LO generation, and a low-frequency delay line for beamforming phase-shift operation. Fabricated in 28-nm CMOS technology, the prototype exhibits a minimum noise figure of 4.7 dB, LO jitter of 215 fs_{rms}, and a phase resolution of 7°. The single element occupies 1.1 mm x 0.9 mm of area and draws 40 mA of current from a 1-V supply.**

***Keywords*—RF path, LO path, amplifier, LNA, Mixer, QVCO, CTLE, Gain, NF, PLL, jitter, delay line, subsampling, phase shifting, beamforming.**

I. Introduction

For 6G radios to find traction in the consumer market, both their power consumption and cost must outperform those of Wi-Fi, at least if normalized to the data rates. Wi-Fi 7 targets 30 Gbps, presenting a tough competition. Extensive work on 140-GHz receivers has improved the performance [1]- [5]. For example, [3] has reduced the power per element to 98 mW while containing no on-chip phase shift, performing digital beamforming off the chip, and also requiring a 2.9-GHz external reference for LO generation. While, RF phase shifting offers the possibility of true time delay [4], we opt for phase shift in the LO path and improve the NF so as to overcome the ISI due to nonlinear phase dependence.

We describe a receiver with a minimum NF of 4.7 dB that draws 40 mW and, requires only a 250-MHz reference frequency while providing a phase shift range of more than 180°in each beamforming element. This performance is achieved by several new techniques: (1) an RF path with low-impedance interfaces to ease the noise-stability trade-off, (2) a 94-GHz subsampling PLL, (3) a new quadrature LC QVCO, and (4) a new phase shift technique that resides at low frequencies and does not degrade the RF and LO paths. Moreover, the RX and its dedicated PLLs occupy a total area of 1.1 mm x 0.9 mm in 28-nm CMOS technology, offering a low-cost compact solution. In addition to the architecture and circuit concepts proposed below, this work reduces the power by avoiding three types of circuits, namely, buffers, passive power splitters, and passive frequency multipliers.

II. Architecture Overview

The RX architecture is dictated by LO path limitations: it is difficult to (a) generate I/Q LO phases at 140 GHz, and (b) divide 140 GHz robustly. We thus propose the heterodyne approach shown in Fig. 1, where the RF signal is first mixed with f_{LO1} = 94 GHz, delivering an IF component that is next mixed with the quadrature phases of f_{LO2} = 47 GHz. Several aspects of this RX distinguish it from the prior art. First, due to the droop in the RF mixer output frequency response, we employ continuous-time equalizers (CTLEs) in the baseband to provide 6 dB of boost at 5 GHz. Second, unlike typical sliding-IF receivers, our architecture doubles the second LO frequency by means of a subsampling PLL (PLL_2) (rather than divide the first one by 2), obviating the need for dividers operating at 94 GHz. This is because the limited speed of 28-nm technology yields a narrow lock range for such dividers, potentially posing a risk to the entire system. Third, the phase shift network necessary for beamforming is embedded in the feedback path of PLL_1, drawing less than 0.5 mW. Fourth, the dedicated LO generation network requires only a 250-MHz reference to be distributed to the beamforming elements on one or multiple chips. Fifth, the absence of inductor-hungry buffers between PLL_1 and PLL_2 and their respective mixers greatly simplifies the floorplan and affords shorter interconnects.

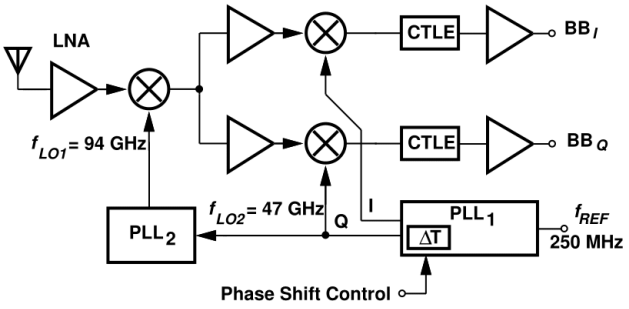


Fig. 1: Proposed 140-GHz receiver architecture.

III. RF Signal Path Architecture

Most D-band LNAs incorporate an input balun along with differential capacitive neutralization of C_{GD} [1] [3] while incurring a noise penalty due to the balun's loss. We should point out that the use of C_{GD} neutralization in two cascaded stages entails two drawbacks: (1) uncertainty in the load impedance of the second stage propagates back to the input of the first stage, degrading the stability, and (2) departure of the neutralization capacitors from their ideal values has a greater impact on stability and gain flatness in the two stages. For these reasons, we wish to apply neutralization to a single stage. It is preferable to use an inductively-degenerated CS

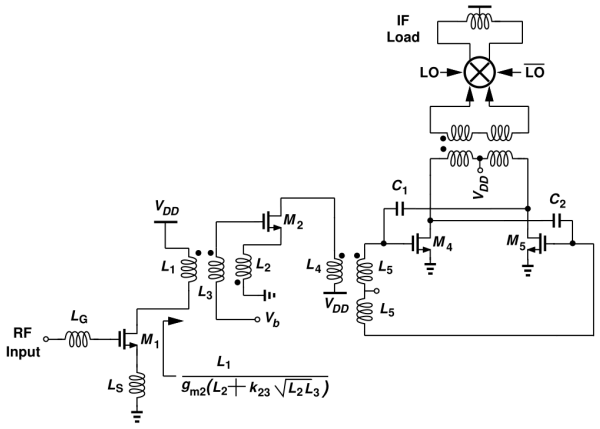
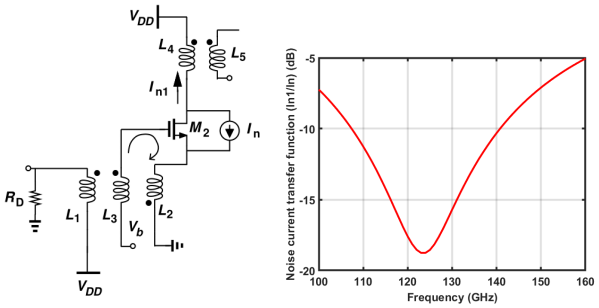


Fig. 2: Receiver front end.



(a) (b)

Fig. 3: SE second stage and transistor noise transfer function.

amplifier as the first stage for low noise, but C_{GD} proves problematic unless the drain is terminated to a low impedance. Since a cascode structure suffers from a low gain in 28-nm technology, we instead tie the drain to a magnetically-coupled CS/CG stage (Fig. 2). It can be shown that the drain of M_1 sees a real impedance equal to the expression depicted in Fig. 2, where k_{23} denotes the coupling factor between L_2 and L_3. This impedance is about 100 Ω in our design. The second stage is differential but shown in single-ended form for the sake of clarity.

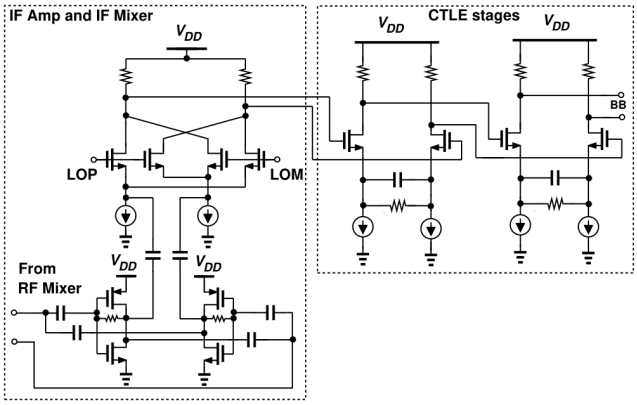


Fig. 4: Receiver IF and BB path.

Another remarkable property of this topology is that the noise current of M_2 flows through L_2, couples to L_3, and changes the gate voltage in the opposite direction [Fig. 3(a)]. That is, the noise of M_2 is partially cancelled, a property that evidently has not been recognized in prior work. Fig. 3(b) demonstrates this phenomenon. This second stage also provides gain boosting. The total voltage gain from the RF input to the drain of M_2 in Fig. 2 is 27 dB. To ensure that the RF mixer's G_m devices (M_4 and M_5) remain stable, we add the balun consisting of L_4 and L_5 and neutralization capacitors C_1 and C_2.

The IF mixer and baseband equalizer stages are depicted in Fig. 4. The mixer transconductors are formed by neutralized self-biased inverters, thus compensating the loss by 5 dB from mixer switching stages. The tank serving as the RF mixer load in Fig. 2 poses a trade-off between the gain and the IF bandwidth. We favor the former and correct the latter by the baseband CTLEs. The entire RX path consumes only 23 mW.

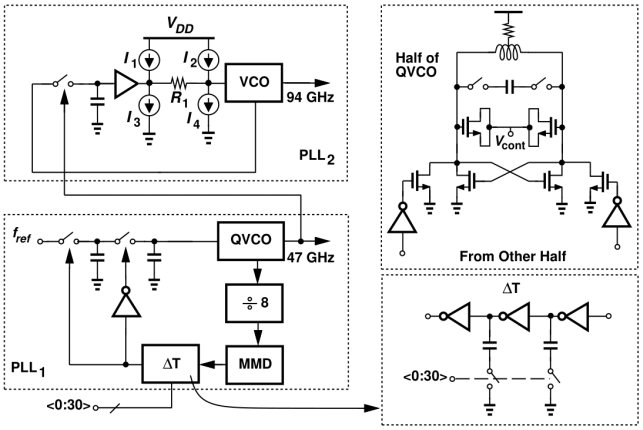


Fig. 5: Proposed LO path architecture.

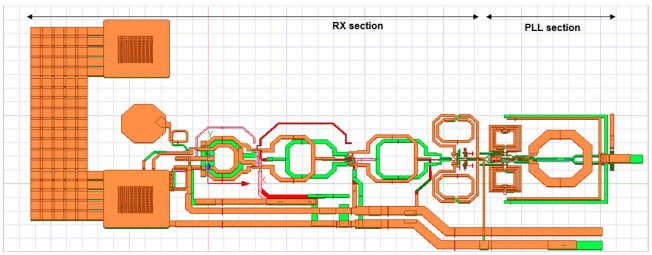


Fig. 6: EM structure of RX and PLL.

IV. LO Path Architecture

A. 94-GHz PLL

The LO generation network in Fig. 1 employs a subsampling structure for PLL_2. The 94-GHz VCO in PLL_2 must double the 47-GHz LO and provide differential waveforms to the double-balanced RF mixer with no intervening buffers. Shown in Fig. 5, the subsampling topology directly ties the output of the VCO to the sampler then applies the result to a programmable dc level shift equal to $-I_1R_1$ (= $-I_4R_1$) or $+I_2R_1$ (= $+I_3R_1$). Since the subsampling architecture exhibits a limited capture range, we insert this level shifter to widen the lock range, a new technique that distinguishes this work from [6]. The

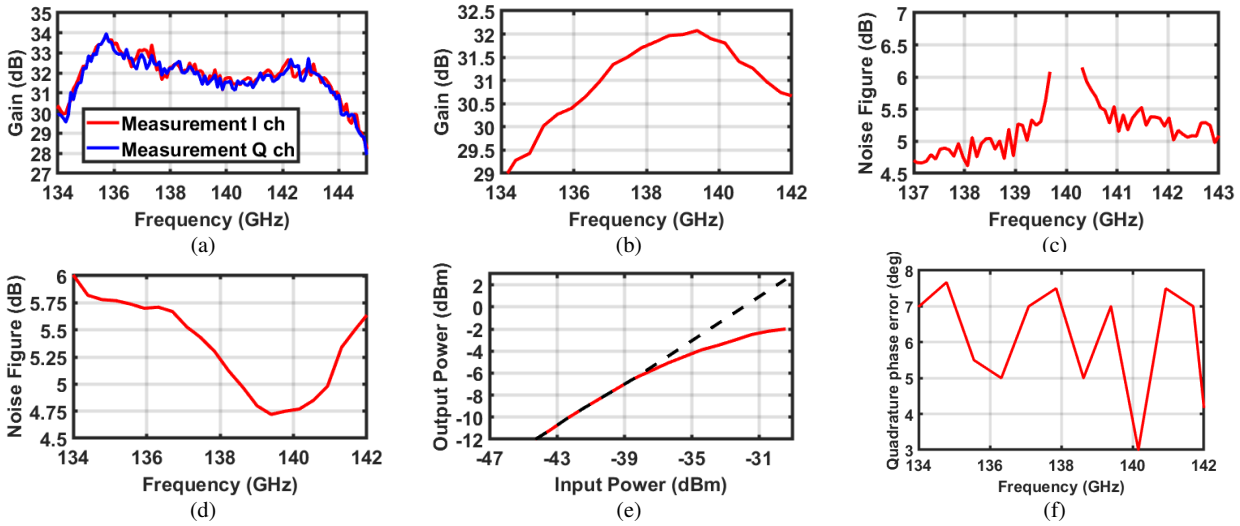


Fig. 7: Measured signal path performance: Gain, NF, compression, and quadrature error.

94-GHz VCO is realized as an LC oscillator with varactor and switched-capacitor tuning. The free-running phase noise is -108 dBc/Hz at 10-MHz offset, which, by virtue of a loop bandwidth of 700 MHz, becomes negligible compared to the reference phase noise.

B. 47-GHz PLL

Operating with f_{REF} = 250 MHz, PLL_1 in Fig. 5 provides quadrature outputs as well as a variable phase shift for beamforming. Shown in Fig. 5, the proposed PLL employs a sampling PD, a QVCO, a ÷ 8 chain, a multimodulus divider (MMD), and a phase-shift network. As shown in Fig. 5, the new QVCO consists of two coupled cores but with inverters inserted in the coupling paths, reduces the phase noise by 6 dB and resolves the mode ambiguity observed in conventional QVCOs. The overall performance of the RX and LO generation was simulated based on the EM structure shown in Fig. 6.

C. Phase Shift for Beamforming

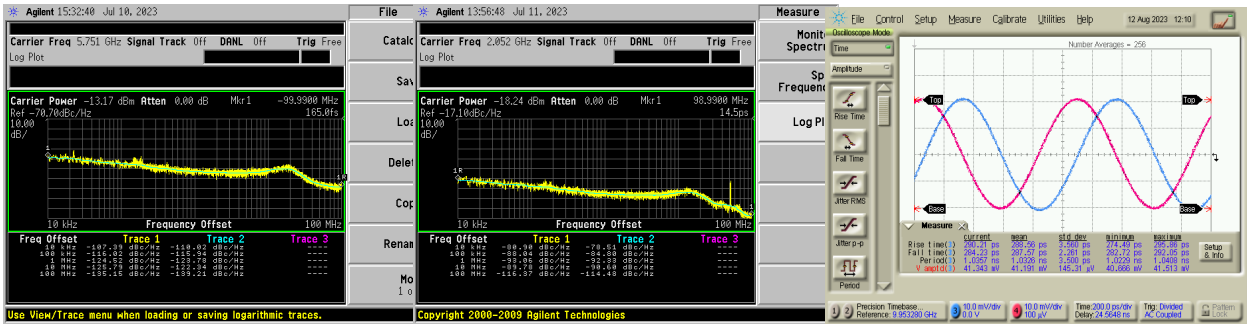
Our per-element LO generation approach provides much more flexibility in the implementation of the phase shift network. Realized by programable-delay stages in Fig. 5, ΔT changes in steps of 150 fs and covers a range of 4.5 ps. These values translate to an overall phase resolution of 7°and a range of slightly more than 180°at 140 GHz. Another jump of 180°can be realized by simply swapping the analog baseband output. Our proposed phase shift technique offers several benefits. First, it avoids the loss-phase-shift trade-offs encountered in the RF or LO paths. Second, it has no effect on the signal path's gain. Third, it operates at low frequencies, consuming 0.5 mW and producing an rms jitter of 15 fs.

V. Experimental Results

The system in Fig. 1 is fabricated in 28-nm CMOS technology. Fig. 10 shows the die photograph. The power breakdown is as follows: 14 mW in the LNA and RF mixer, 9 mW in the IF mixers and baseband chains, 11 mW in PLL_1, and 6 mW in PLL_2. The signal path performance has been characterized by probe testing where VDI's KT-8257DV08 provides a 140 GHz input through waveguides. A VDI Erickson power meter (PM5B) is used to measure the input power to the probe.

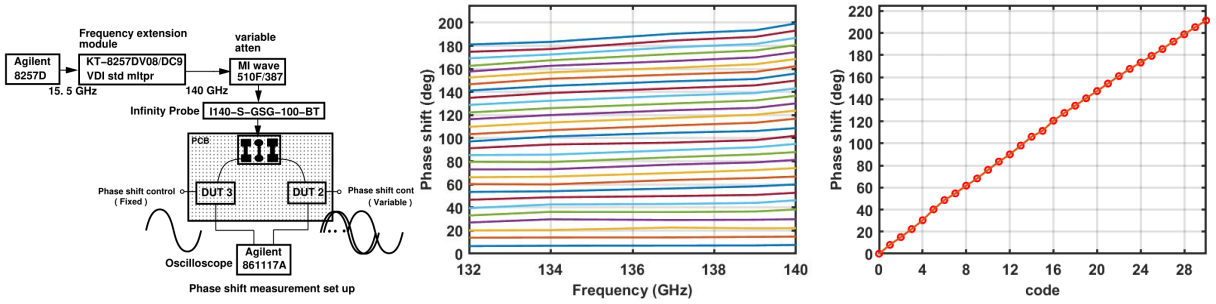
A. RF Signal Path Performance

Fig. 7 plots the measured signal path characteristics. The gain is measured for a fixed LO frequency, indicating a channel



(a) (b) (c)

Fig. 8: (a) Phase noise of PLL_1 after division by 8, (b) and phase noise of RX downconverted signal in baseband, and (c) and baseband IQ time domain waveform.



(a) (b) (c)

Fig. 9: (a) Phase shift measurement set up, (b) measured phase shift vs input frequency for all codes, (c) and phase shift vs code at 140GHz.

BW of 10 GHz in Fig. 7(a). The close agreement with the simulated gain of 33.5dB confirms proper LO swings provided by the two PLLs. The RF bandwidth for this design is 10 GHz when the gain is measured at fixed IF of 1 GHz is shown in 7(b). The NF (DSB) is measured for a fixed LO frequency [Fig. 7(c)] or a fixed baseband frequency [Fig. 7(d)]. The NF varies between 4.75 dB and 6 dB, the lowest reported for D-band receivers. The NF is measured in two steps: (1) the RX output noise floor is displayed on a low-noise spectrum analyzer, (2) this flore is divided by the measured gain and compared with 50 Ω to obtain the SSB NF. The baseband quadrature phase error ranges from 4°to 7.2°, and the RX output P1dB is equal to -4 dBm.

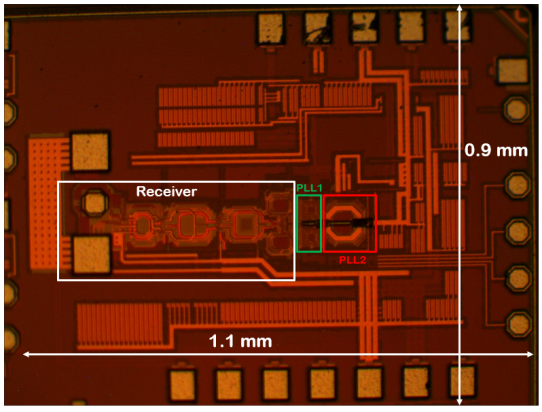


Fig. 10: Die photo of single element Receiver with integrated PLL.

B. LO Path Performance

Fig. 8 plots the measured LO path characteristics. The lock ranges of PLL_1 and PLL_2 are 4.5 GHz and 9 GHz, respectively. PLL_1 in Fig. 5 provides an output after the ÷ 8 stage, yielding the phase noise profile shown in Fig. 8(a). The PN reaches a plateau of about -120 dBc/Hz and, integrated from 10 kHz to 100 MHz, gives an rms jitter of 165 fs. The contributions of both PLL_1 and PLL_2 are captured by monitoring the baseband output, which exhibits the PN shown in Fig. 8(b). A jitter of 14.5 ps for the downconverted 2.052-GHz baseband frequency corresponds to 215 fs at 140 GHz. No pulling between the two PLLs has been observed, nor false lock in the subsampling PLL.

	This work	Li JSSC' 22 [1]	Elkholy ISSCC' 22 [2]	Chou ESSCIRC' 22 [3]	Karakuzulu JSSC' 23 [4]	Agrawal ISSCC' 23 [5]
Tech. (nm)	28–nm CMOS	45–nm CMOS SOI	135–nm SiGe	28–nm CMOS	130–nm BiCMOS	22–nm FinFET
Frequency (GHz)	130 –145	139 –155	130 –164	135	110–170	140
Channel BW (GHz)	10	3.5 – 4.5	N/A	10	60	N/A
Number of Elements	1	8	4 – 1024	4	4	1
Beamforming Architecture	Low–Frequency Delay Line	IF Beamforming	RF Beamforming	External Digital Beamforming	RF Beamforming	No Beamforming
Area (mm^2)	0.9 per RX element	3.11 per RX element	0.9 per TRX element	1.2 per RX element	6.8 per TRX element	0.7 per RX element
NF (dB)	4.7	6.4	7.5	7.8	10.08	12.4
Gain (dB)	32	27.5	30	58	22	15
On–Chip I/Q Gen	Yes	NO	NO	Yes	Yes	Yes
Power per Element (mW)	40	145	200	98	487	123
Phase Resolution (deg)	7	11.25	2	Not applicable	22.5	Not applicable
REF Frequency	250 MHz	21–24 GHz	N/A	2.9 GHz	35 GHz	5.8 GHz
Integrated Jitter	215 fs	N/A	N/A	N/A	N/A	N/A

· Minimum noise figure across the bands.

Table 1: Performance summary and comparison.

C. Phase-Shift Network Performance

The programable phase shift for beamforming is measured by examining the baseband outputs of two RX chips driven simultaneously by the same D-band source [Fig. 9(a)]. Shown in Fig. 9(b) and (c) is the phase shift vs the input frequency and vs the code. The phase varies fairly linearly in both cases.

Table 1. summarizes the measured performance and compares it to the prior art.

VI. Conclusion

The use of new concepts such as low-impedance RF interfaces, subsampling PLLs as multiplying-by-2 stages, and a reference phase shift network lead to a self-contained beamforming RX element that achieves the highest performance reported to date.

References

[1] S. Li et al., "An Eight-Element 140-GHz Wafer-Scale IF Beamforming Phased-Array Receiver With 64-QAM Operation in CMOS RFSOI," *IEEE J. Solid-State Circuits*, 2022.

[2] M. Elkhouly et al., "Fully Integrated 2D Scalable TX/RX Chipset for D-Band Phased-Array-on-Glass Modules," *IEEE ISSCC Dig. Tech. Papers*, 2022.

[3] E. Chou et al., "A Low-Power and Energy-Efficient D-Band CMOS Four-Channel Receiver with Integrated LO Generation for Digital Beamforming Arrays," *IEEE ESSCIRC*, 2022.

[4] A. Karakuzulu et al., "A Four-Channel Bidirectional D-Band Phased-Array Transceiver for 200 Gb/s 6G Wireless Communications in a 130-nm BiCMOS Technology," *IEEE J. Solid-State Circuits*, 2023.

[5] A. Agrawal et al., "A 128Gb/s 1.95pJ/b D-Band Receiver with Integrated PLL and ADC in 22nm FinFET," *IEEE ISSCC Dig. Tech. Papers*, 2023.

[6] O, memioglu et al., "A 300GHz 52mW CMOS Receiver with On-Chip LO Generation," *IEEE ISSCC Dig. Tech. Papers*, 2022.