A Layout Technique for Millimeter-Wave PA Transistors[1]

ChuanKang Liang and Behzad Razavi
Electrical Engineering Department
University of California, Los Angeles, CA 90095

Abstract—The distributed interconnect parasitics within large transistors markedly degrade the output power and efficiency at millimeter-wave frequencies. This paper develops a model for such structures and proposes a layout technique to reduce the effect of source terminal parasitics. The technique is applied to a 60-GHz prototype in 65-nm CMOS technology, raising the output power from 5 to 10 dBm and the drain efficiency from 3.7% to 10.7%.

***Index Terms*—Millimeter-wave power amplifier, layout technique, distributed parasitics, source parasitics, power efficiency.**

I. Introduction

The problem of layout parasitics assumes new dimensions in millimeter-wave power amplifiers (PAs) realized in deep-submicron CMOS technologies. With narrow, thin metal layers serving as source and drain wires, both the resistance and inductance of interconnects can drastically degrade the output power and efficiency of these circuits. For example, a transistor carrying a peak current of 40 mA at 60 GHz experiences severe degeneration with a source inductance of only 5 pH. (corresponding to roughly a 5-μm-long line). With CMOS 60-GHz PAs approaching output levels of 15 to 20 dBm [1-3], even higher currents must be handled, making the problem of interconnect parasitics more serious.

This paper describes a layout technique for differential pairs that considerably reduces the adverse effects of interconnect resistance and inductance on the performance of PAs. Incorporated in a 60-GHz 65-nm CMOS prototype, the technique increases the output power from 5 dBm to 10 dBm and the drain efficiency from 3.7% to 10.7%.

Section II deals with the modeling of mm-wave interconnects in PAs and quantifies their effect on the performance. Section III describes the proposed structure and compares its performance with that of the conventional layout. Section IV presents the experimental results.

II. Effect of Distributed Parasitics

At high frequencies and high current levels, interconnect parasitics require that large multi-finger transistors be viewed as distributed structures. In this section, the effect of distributed parasitics in the source, gate, and drain terminals of MOSFETs is quantified and an equivalent lumped model is developed.

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A. Source Parasitics

Consider the "linear" multi-finger transistor structure shown in Fig. 1(a). The wire tying the source terminals reaches ground at one end, introducing a distributed impedance in the source network with a unit value of Z_u. We wish to derive a lumped model for this structure. Drawing the equivalent circuit as shown in Fig. 1(b)[2] and noting that in a well-designed layout, the unit drain currents are roughly equal, we write the voltage at source number j as:

$$V_j = NI_1Z_u + I_1Z_u\frac{(2N-j)}{2}(j-1). \quad (1)$$

Thus, unit transistor number j experiences a current reduction given by $\Delta I_j = g_{m,u}(V_j - V_1)$. For ΔI_j to be much less than I_1, we must have $g_{m,u}Z_u(N^2/2 - N/2) \ll 1$.

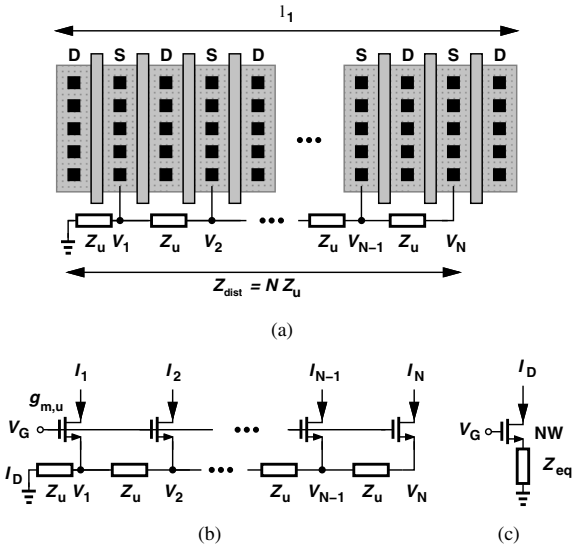

Fig. 1. (a) Multi-finger transistor structure, (b) distributed model, and (c) equivalent lumped model.

To determine the lumped equivalent of the above structure, we consider the topology of Fig. 1(c) and seek the condition under which its transconductance is equal to that of the distributed device in Fig. 1(b). For a small-signal gate voltage of V_G in Fig. 1(b), it can be shown that

$$\begin{aligned} I_1 + \cdots + I_N &= NI_1 - \sum_{j=1}^{N}\Delta I_j \\ &= \frac{Ng_{m,u}}{1+Ng_{m,u}Z_u}(1 - g_{m,u}Z_u\frac{2N^2-3N+1}{6})V_G. \end{aligned}$$

[2]Each transistor represents two fingers.

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Since $g_{m,u}Z_uN^2/2 \ll 1$, this equation simplifies to

$$\begin{aligned} I_1 + \cdots + I_N &\approx Ng_{m,u}(1 - g_{m,u}Z_u\frac{N^2}{3})V_G \\ &\approx \frac{Ng_{m,u}}{1 + Ng_{m,u}\frac{NZ_u}{3}}V_G. \end{aligned} \quad (2)$$

This result represents a lumped transistor having a width of NW and a transconductance of $Ng_{m,u}$ and degenerated by a source impedance of $Z_{eq} = NZ_u/3$. That is, the distributed source impedance is simply divided by a factor of 3, as is the distributed gate resistance [4].

The above analysis neglects the effect of distributed gate wiring impedance and the gate ac current. This is a rough approximation because at 60 GHz and with an f_T of about 180 GHz, the gate current is several times smaller than the source current.

To relate the foregoing results to a practical case, we consider a 60-GHz PA example that employs an NMOS transistor with W/L =96 μm/60 nm and a bias current of 84 mA. Figure 2 plots contours of constant output power degradation as a function of the total (lumped) resistance and inductance in series with the source. It is observed that, for a 0.5-dB degradation, the maximum tolerable lumped resistance and inductance are, e.g., equal to 1 Ω and 1 pH, respectively.

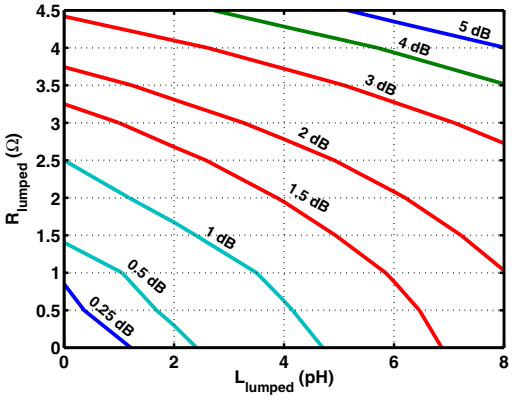


Fig. 2. Output power degradation for lumped resistance and inductance values in the source.

Another important point revealed by Eq. (2) is that, as the number of fingers, N, increases, the overall transconductance rises, reaches a maximum, and *falls* thereafter (Fig. 3). For example, if $g_{m,u} = (300\ \Omega)^{-1}$ and $Z_u = 0.6\ \Omega$ (at 60 GHz), then $N_{max} \approx 40$, suggesting that the number of fingers must be kept *well below* this value to avoid waste of current. In reality, the assumption $I_1 \approx I_N$ in Fig. 1(b) fails for large N, and the transconductance exhibits the saturating behavior shown in Fig. 3.

B. Drain and Gate Parasitics

The "1/3 rule" developed above for a linear array of fingers can also be applied to the drain and gate parasitics. As illustrated in Fig. 4(a), each finger and its interconnects are represented as one unit in the distributed model. Note that the capacitances shown here denote the *extrinsic* components

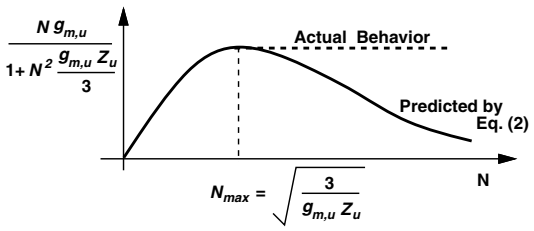


Fig. 3. Device transconductance as a function of the number of fingers.

arising from the metal layers atop each finger [5]. For N such units, the equivalent lumped model appears as in Fig. 4(b).

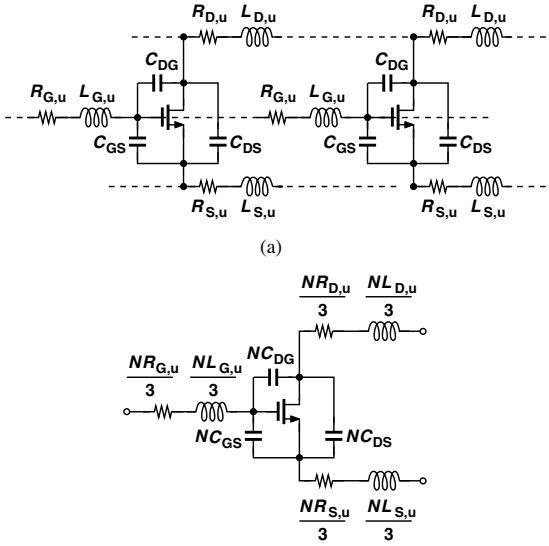


Fig. 4. Distributed and lumped models of a multi-port structure.

C. Layout Issues

From the study in the previous section, we conclude that a 96-μm device must incur no more than 3 Ω and 3 pH of distributed parasitics in its source network. This constraint demands that *wide* gate fingers be used such that the total lateral dimension, l_1 in Fig. 1(a), is minimized. Since the gate resistance limits the performance for wide fingers, a compromise must be sought. In this work, each finger has a width of 1.2 μm (20 squares), leading to l_1 = 21 μm for a total width of 96 μm. The distributed resistance, R_{dist}, and inductance, L_{dist}, associated with such a source line are much greater than the tolerable values mentioned above. (Field simulations indicate R_{dist} = 8.8 Ω and L_{dist} = 13.4 pH at 60 GHz).

The above issue is alleviated by folding the device into two linear structures so as to halve the lateral dimension (Fig. 5). However, a *differential* PA using two such devices must deal with a relatively long *vertical* dimension, l_2 (≈10 μm).

III. Proposed Technique

We propose an "interleaved" layout technique for differential pairs that converts the source degeneration network seen

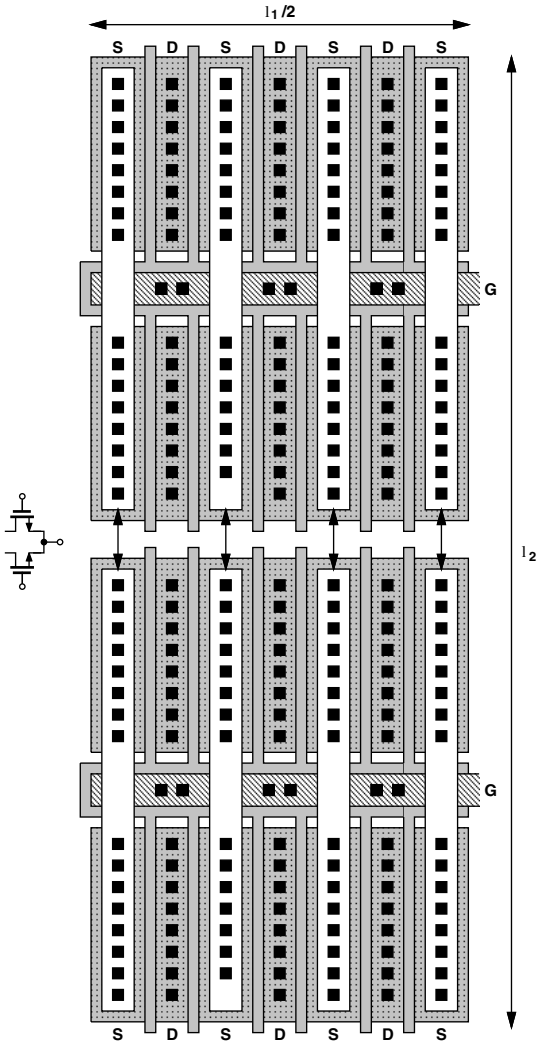


Fig. 5. Conventional differential pair layout.

by each transistor to a common-mode impedance. Figure 6(a) illustrates the concept: a unit cell consisting of two gate fingers of each transistor is formed by overlapping two of the four source areas, and adjacent unit cells also have overlapping source areas. As a result, each source junction carries the sum of two differential currents, and the interconnect parasitics manifest themselves as a common-mode degeneration network.

Figure 6(b) illustrates the transformation provided by this technique: since the source terminals now carry only common-mode currents, the interconnect parasitics do not affect the differential operation.

Another key advantage of the proposed structure is that it can also be duplicated in the vertical dimension with less concern for the length of the vertical interconnects. As shown in Fig. 6(c), l_2 is less critical here than in Fig. 5 because each internal source junction carries only a common-mode current, and so do vertical lines tying the sources to one another. This flexibility leads to a more square layout and hence shorter

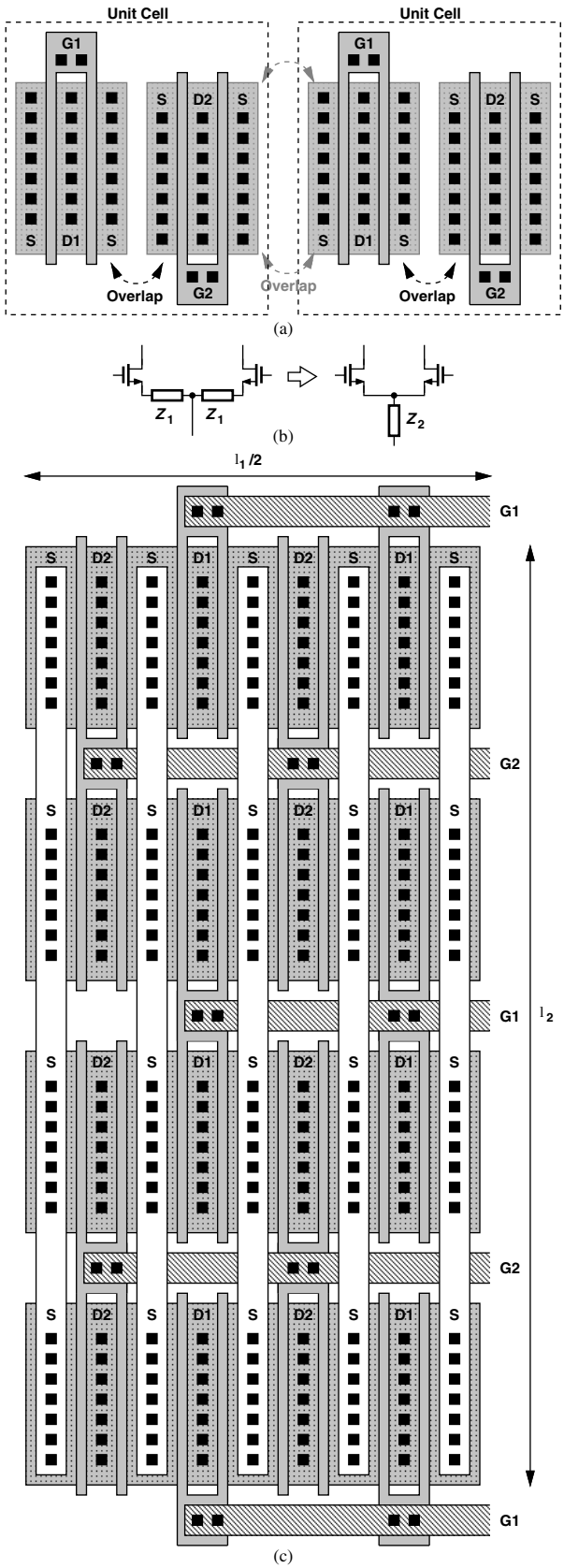


Fig. 6. (a) Unit cells in proposed structure, (b) transformation of the degeneration impedances, and (c) combined cells in a complete differential pair.

interconnects. For example, the 96-μm device can be laid out in an area of 8.4 μm$\times$7.5 μm.

IV. Experimental Results

In order to evaluate the power delivery capability of differential pairs, we propose to configure them as an *oscillator*. Shown in Fig. 7, such a topology allows a fair comparison of the layout techniques described above with no need for an input network. The on-chip balun is constructed as a stack of metal 9 and metal 8 one-turn spirals. The load inductors provide a low-resistance path in parallel with the balun's primary, reducing the dc voltage drops that result from high bias currents. The circuit is designed in 65-nm technology.

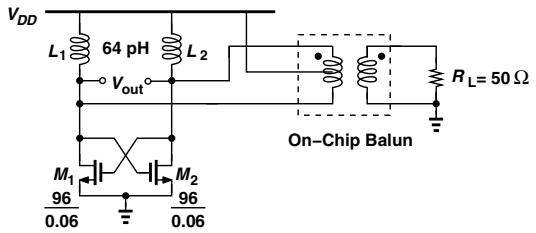
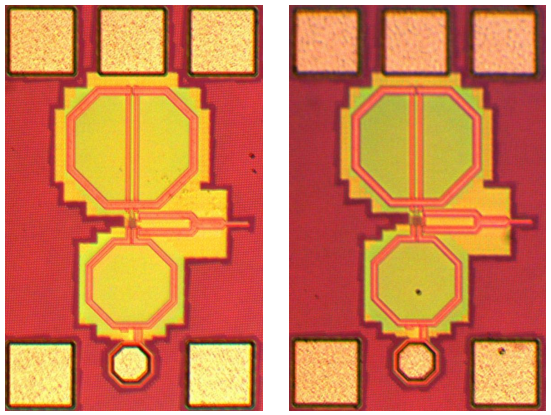


Fig. 7. Prototype circuit.

Figures 8(a) and 8(b) show the die photographs of the two prototypes employing the layout technique of Figs. 5 and 6(c). Except for the transistor layouts, all other parameters are the same. Each chip occupies an area of 400 μm$\times$450 μm. The circuits have been tested on a probe station, with the output power measured by a V-band power meter.

Table I summarizes the performance of the two prototypes. The proposed scheme leads to a slightly larger bias current and higher frequency due to the more square layout. In addition, the output power provided in the proposed layout is 4.9 dB higher, demonstrating significant improvement as a result of shared source diffusions of the differential pair.

Figures 9 and 10 plot the measured output power and efficiency of the two circuits as a function of the supply voltage. It is observed that the proposed technique raises the output power by as least 4.9 dB and the drain efficiency from 3.7% to 10.7%.



(a) (b)

Fig. 8. Prototype die photos with (a) the conventional layout and (b) the proposed layout.

TABLE I

	Proposed	Conventional
Frequency	59.5 GHz	58.6 GHz
Output Power	10.1 dBm	5.2 dBm
DC Current	95.3 mA	88.1 mA
Supply Voltage	1 V	1 V
Drain Efficiency	10.7 %	3.7 %

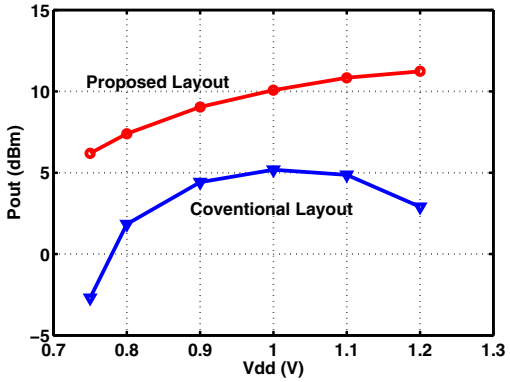


Fig. 9. Measured output power with conventional and proposed techniques.

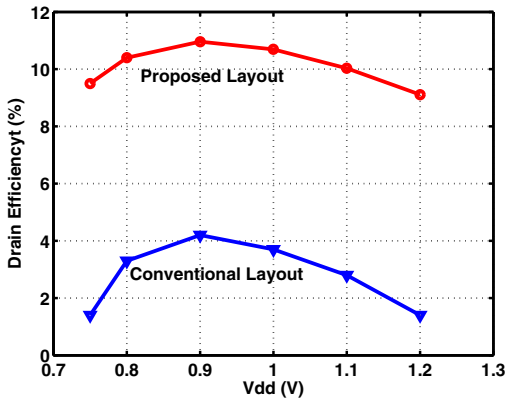


Fig. 10. Measured drain efficiency with conventional and proposed techniques.

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