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Fifty Applications of the CMOS Inverter—Part 4

In this article series, we have studied the use of the CMOS inverter in various analog and digital systems. As mentioned in the previous installments, the low supply voltages imposed by modern CMOS processes have made the inverter attractive for realizing circuit functions. In this article, we examine more topologies and quantify their performance in the slow–slow corner of 28-nm technology with $V_{DD} = 95$ V and at $T = 75$ °C.

The Physically Unclonable Function

In some applications, especially where hardware security is of concern, it is necessary to assign a unique identification number to every chip that is manufactured and sold. Also called a "physically unclonable function" (PUF) the ID can be realized by on-chip "fuses" that are programmed during testing but at an additional cost. To avoid fuses, a clever approach was introduced by [1] that exploited variabilities in MOSFETs. The arrangement is shown in Figure 1.

To understand the essence of the idea, let us consider the simplified cascade depicted in Figure 2(a), where the first and second stages have the same bias voltage, V_b, e.g., $V_b \approx V_{DD}/2$. Due to random variations in the properties of M_1 and V_1, V_1 exhibits a Gaussian distribution, $f_V(V_1)$, around V_b with a certain standard distribution (SD), σ_{V1}. For

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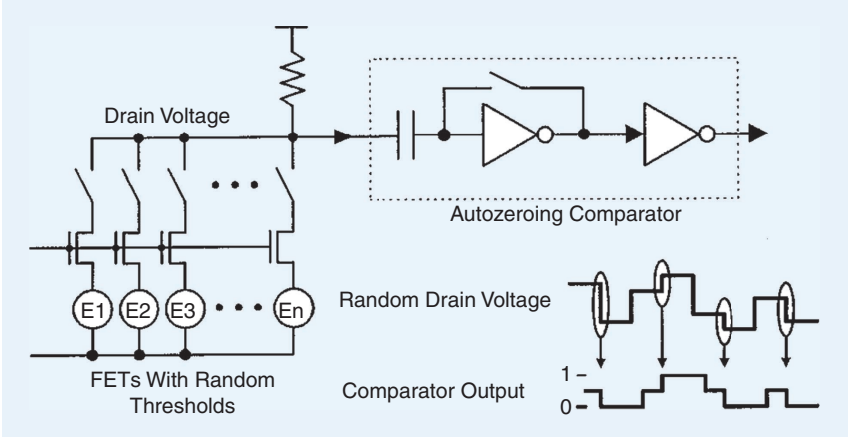

FIGURE 1: A PUF circuit reported in the year 2000.

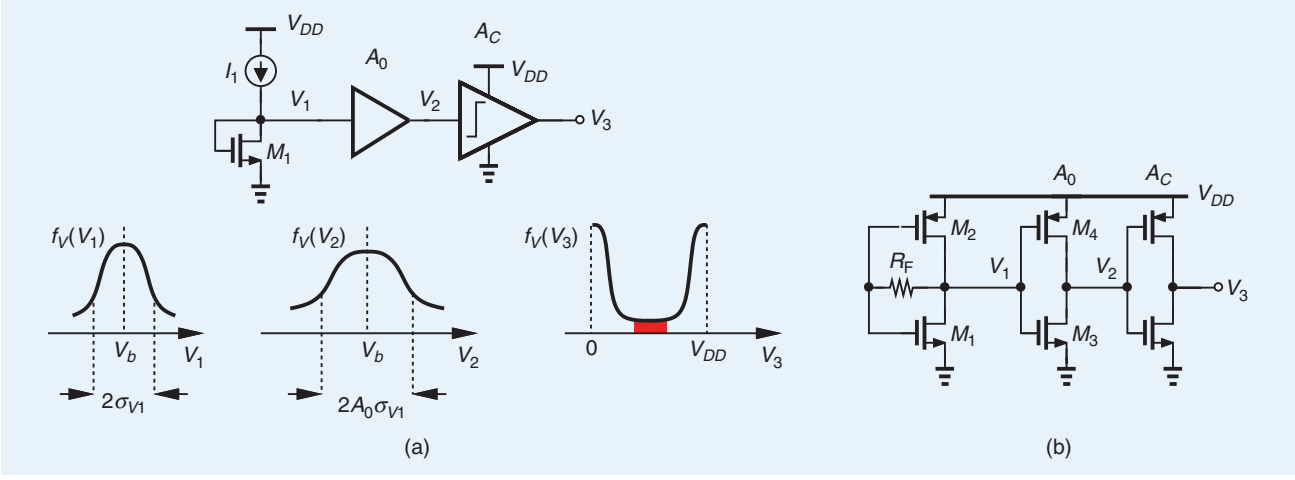

FIGURE 2: (a) A conceptual realization of the PUF and (b) its inverter-based topology.

example, $\sigma_{V1} = 10\,\text{mV}$. Upon traveling through amplifier A_0, V_1 yields V_2, with an SD equal to $\sigma_{V2} = A_0\sigma_{V1}$. For example, $\sigma_{V2} = 100\,\text{mV}$. Note that the peak of $f_V(V_2)$ is lower, as if the new distribution were flatter.

Now, suppose V_2 drives a comparator, A_C, realized simply as a high-gain, limiting amplifier. For example, if $A_C = 20$ and $V_{DD} \approx 1$ V, any $|V_2 - V_b|$ greater than 0.5 V/20 = 25 mV yields an output, V_3, equal to V_{DD} or zero. Ideally, this occurs with 50% probability, producing a random 1-bit output. An array of m such cascades thus provides an m-bit ID for each chip.

An efficient realization of this idea is depicted in Figure 2(b) [2], with the first stage defining the bias, V_b, to be the trip point of the inverters. In this case, the random variations in V_1 arise from both M_1 and M_2.

The arrangement of Figure 2(a) entails a number of issues. First, if V_1 departs by a small amount from V_b, then $A_0A_C|V_1 - V_b|$ may not reach V_{DD} or zero, presenting an ambiguous logical level. For example, if $A_0A_C = 200$, samples in which $|V_1 - V_b|$ is less than 0.5 mV occupy the red region in $f_V(V_3)$. That is, a fraction of chips fail to attain a proper ID.

Second, suppose in Figure 2(b), $V_1 = V_b + \Delta V$ and $\Delta V > 0$. We expect V_2 to be less than V_b and V_3 to reach V_{DD} if A_0A_C is sufficiently large. But M_3 and M_4 exhibit their own random variations, possibly yielding $V_2 > V_b$ and $V_3 \approx 0$. While this effect is benign per se, the difficulty is that the "error" in V_3 due to M_3 and M_4 varies with temperature, causing the logical value of V_3 also to change [2].

We simulate the circuit of Figure 2(b) with W/L equal to 250 nm/30 nm for M_1 and M_2 and 1 μm/120 nm for the remaining devices. To minimize power consumption and obtain a high voltage gain, we select V_{DD} = 0.6 V so as to bias the transistors in the subthreshold region. We thus have $A_0 \approx A_C \approx 10$. A Monte Carlo simulation yields the distributions of V_1, V_2, and V_3 (Figure 3), implying $\sigma_{V1} = 10\,\text{mV}$. We observe that V_3 assumes a high level with a greater probability, demanding further adjustments to the design. For more details, the reader is referred to [2].

Comparators operate as quantizers in analog-to-digital converters (ADCs) and as sense amplifiers in memories.

The Offset-Canceled Comparator

Comparators operate as quantizers in analog-to-digital converters (ADCs) and as sense amplifiers in memories. Their task is to sense an input difference and

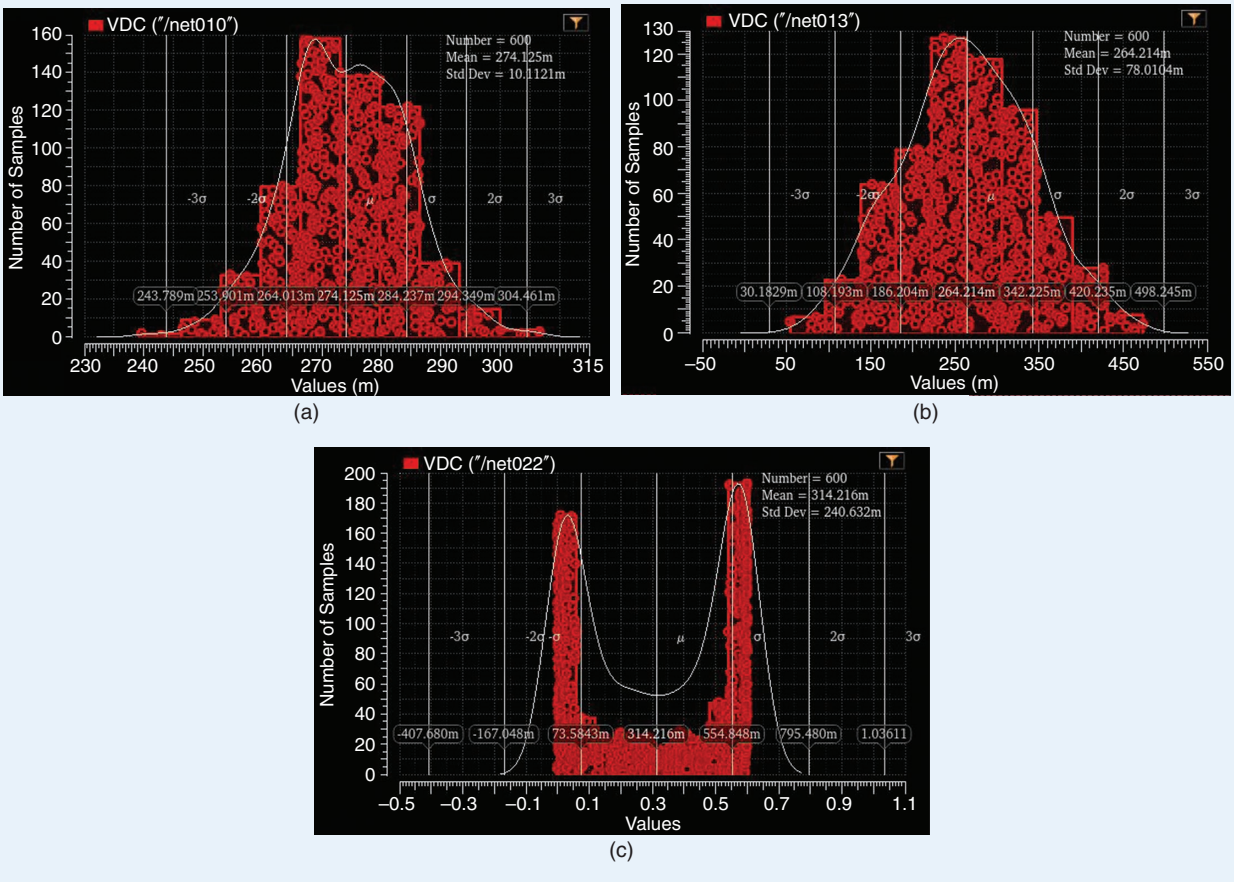

FIGURE 3: Distributions of voltages: (a) V_1, (b) V_2, and (c) V_3.

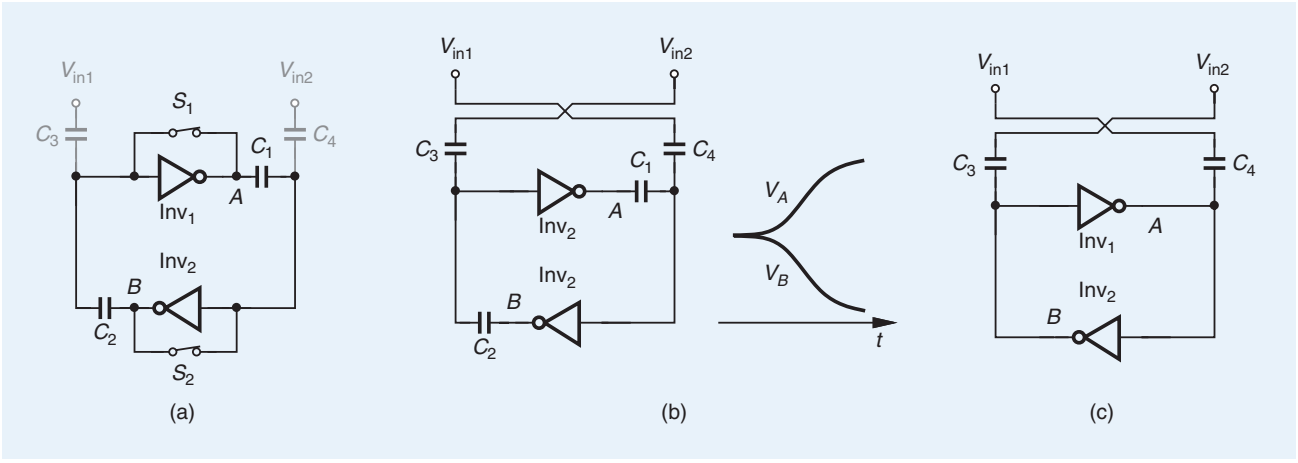

FIGURE 4: The comparator in (a) offset cancelation mode, (b) initial regeneration mode, and (c) final regeneration mode.

regeneratively amplify it to deliver logical levels at the output. The input offset, V_{OS}, of comparators must remain sufficiently small in both applications, often requiring offset cancelation.

Consider the arrangement shown in Figure 4(a) [3], where Inv_1 and Inv_2 are reset and biased at their trip points. The inputs, V_{in1} and V_{in2}, are constant in this mode. Due to mismatches, the dc levels at A and B may not be equal. However, even after S_1 and S_2 are turned off, V_A and V_B remain at their original values (if the switch imperfections are neglected). We observe that the loop is completely balanced and ready to amplify regeneratively even for a small perturbation. That is, the offset is canceled.

We now disengage S_1 and S_2 and swap V_{in1} and V_{in2} [Figure 4(b)]. The input change thus created triggers positive feedback around the loop, allowing V_A and V_B to reach full logical levels. However, capacitors C_1 and C_4 form a voltage attenuator, and so do C_2 and C_3, reducing the loop gain and degrading the regeneration speed. For this reason, we "short out" C_1 and C_2 by switches [Figure 4(c)] and obtain a faster response [3].

The foregoing structure entails a number of issues. First, upon turning off, S_1 and S_2 may inject unequal charges onto the loop and cause it to regenerate even before an input difference is applied. This translates to a large offset. Second, C_3 and C_4 still degrade the speed in Figure 4(c).

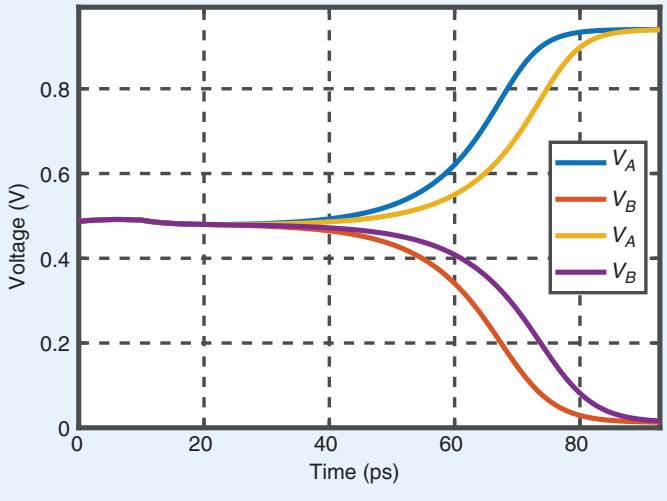

FIGURE 5: Comparator waveforms for 3-mV and 1.5-mV input differences.

We simulate the circuit with $(W/L)_P = (W/L)_N = 2\,\mu$m/30 nm and $C_1 = \cdots = C_4 = 10$ fF. Figure 5 plots the resulting waveforms for an input difference of 3 mV or 1.5 mV. The regeneration time constant is given by the time shift divided by ln2 and amounts to 9.1 ps. The power consumption is 0.18 mW.

As mentioned above, mismatches between the charges injected by S_1 and S_2 initiate false regeneration. Suppose Inv_1 and Inv_2 suffer from mismatches so that their trip points differ by, say, 10 mV. The channel charges of S_1 and S_2 are therefore slightly different due to their unequal gate-source voltages. According to simulations, for the residual offset arising from the false regeneration to remain below 1.5 mV, the input voltage change in Figure 4(b) must occur less than 20 ps after the circuit leaves the offset cancelation mode.

The Continuous-Time Linear Equalizer

We have seen in the first article in this series that inverters can be configured to behave as active inductors, allowing us to construct continuous-time linear equalizers (CTLEs). Another interesting inverter-based CTLE is described in [4]. Consider the topology shown in Figure 6(a), where the lower branch serves as a feedforward path. Here, Inv_1 provides a transconductance equal to G_{m1} and Inv_2 acts as

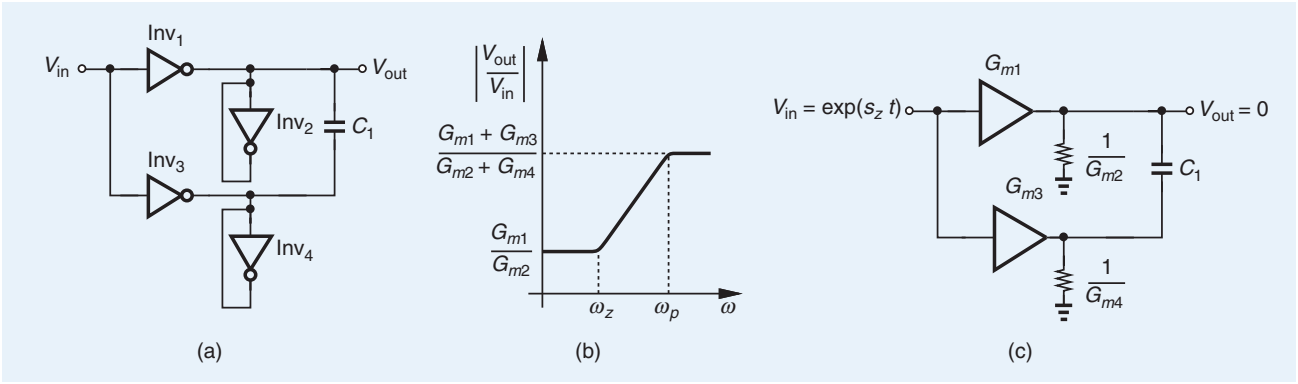

FIGURE 6: (a) A CTLE circuit, (b) its frequency response, and (c) simplified circuit for pole and zero calculations.

a resistance equal to $1/G_{m2}$. This "diode-connected" inverter configuration is necessary to ensure that the transistors in Inv_1 operate in saturation. Similar properties hold for Inv_3 and Inv_4, respectively. Neglecting channel-length modulation, we write the low-frequency gain as

$$\left|\frac{V_{\text{out}}}{V_{\text{in}}}\right|_{\text{LF}} = \frac{G_{m1}}{G_{m2}}. \tag{1}$$

At high frequencies, the capacitor is nearly a short, the output currents of Inv_1 and Inv_3 add, and the result flows through the parallel combination of Inv_2 and Inv_4. Thus,

$$\left|\frac{V_{\text{out}}}{V_{\text{in}}}\right|_{\text{HF}} = \frac{G_{m1}+G_{m3}}{G_{m2}+G_{m4}}. \tag{2}$$

It is possible to select the G_m's so that the gain rises with frequency, thereby creating a boost [Figure 6(b)] equal to

$$B = \frac{G_{m1}+G_{m3}}{G_{m1}}\frac{G_{m2}}{G_{m2}+G_{m4}}. \tag{3}$$

For example, if Inv_1 and Inv_4 are weak and Inv_2 and Inv_3 strong, we have $B \approx G_{m3}/G_{m1}$.

To gain additional insights, we compute the zero and pole frequencies in Figure 6(b). If an input of the form $\exp(s_z t)$ is applied such that $V_{\text{out}} = 0$, then s_z is the zero frequency. In this case, the circuit reduces to that in Figure 6(c), revealing that no current flows through $1/G_{m2}$. We write the voltage across C_1 as $G_{m1}V_{\text{in}}/(C_1 s_z)$ and the current through $1/G_{m4}$ as $[G_{m1}V_{\text{in}}/(C_1 s_z)]G_{m4}$. That is,

$$\frac{G_{m1}V_{\text{in}}}{C_1 s_z}G_{m4} + G_{m3}V_{\text{in}} = -G_{m1}V_{\text{in}} \tag{4}$$

and hence

$$s_z = -\frac{G_{m1}G_{m4}}{(G_{m1}+G_{m3})C_1}. \tag{5}$$

Note that $\omega_z = |s_z|$ and $\omega_p = B\omega_z$. Alternatively, Figure 6(c) suggests that C_1 sees a total series resistance equal to $1/G_{m2} + 1/G_{m4}$, yielding

$$\omega_p = \frac{G_{m2}G_{m4}}{(G_{m2}+G_{m4})C_1}. \tag{6}$$

Remarkably, G_{m4} can scale both ω_z and ω_p.

We should point out that the input dc level in Figure 6(a) must be accurately defined and controlled so as to ensure that Inv_1 and Inv_3 do not incur a large mismatch between their NMOS and PMOS bias currents. Otherwise, the output dc levels may fall or rise excessively, degrading G_{m1} and G_{m3}.

We simulate the CTLE with $(W/L)_P = 2(W/L)_N = 16\ \mu\text{m}/30\ \text{nm}$ for Inv_3, $(W/L)_P = 2(W/L)_N = 2\ \mu\text{m}/30\ \text{nm}$ for Inv_1, and $(W/L)_P = 2(W/L)_N = 1\ \mu\text{m}/30\ \text{nm}$ for Inv_2 and Inv_4. With $C_1 = 25$ fF, we arrive at the frequency response presented in Figure 7. The circuit is also loaded by a capacitance of 20 fF. The CTLE achieves a boost factor of 8 dB at 20 GHz while consuming 1.7 mW.

The Gyrator

A gyrator inverts an impedance, transforming, for example, a capacitor, $1/(Cs)$, to an inductor, Cs. Shown in Figure 8(a) is an example, which can also be reduced to that in Figure 8(b), i.e., a simple active inductor. Note that a net sign inversion is necessary around the feedback loop. The former yields

$$Z_{\text{in}} = \frac{C_1 s}{G_{m1}G_{m2}} \tag{7}$$

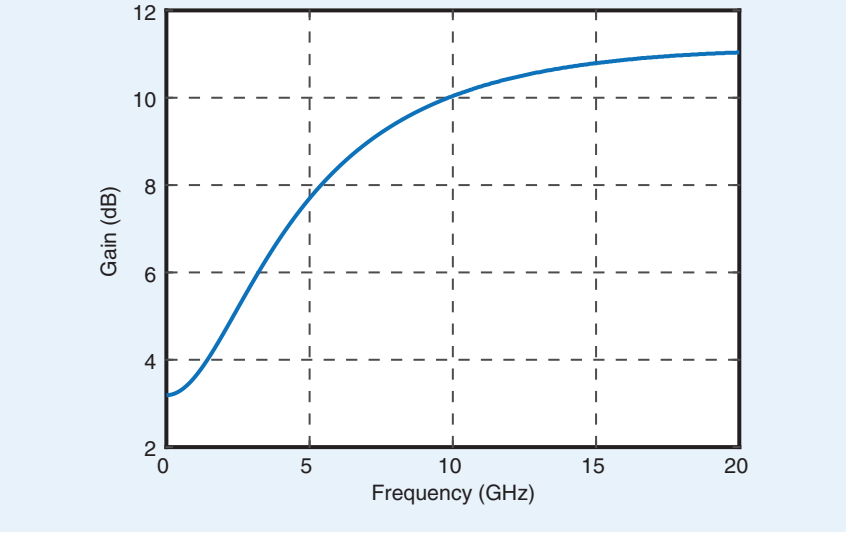

FIGURE 7: Simulated CTLE frequency response.

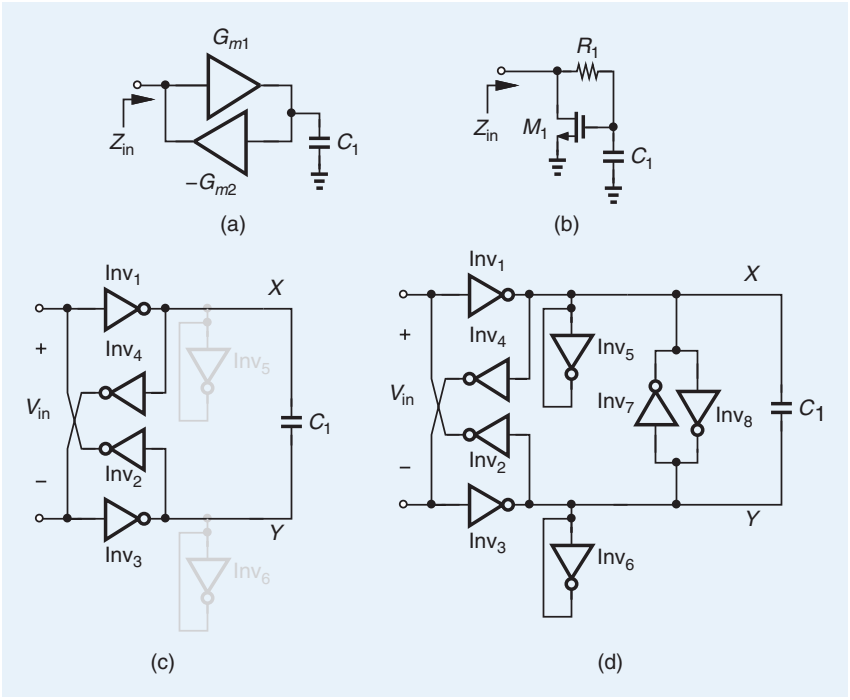

FIGURE 8: (a) A single-end gyrator, (b) its simple implementation, (c) a differential gyrator yielding a large inductance, and (d) the complete circuit.

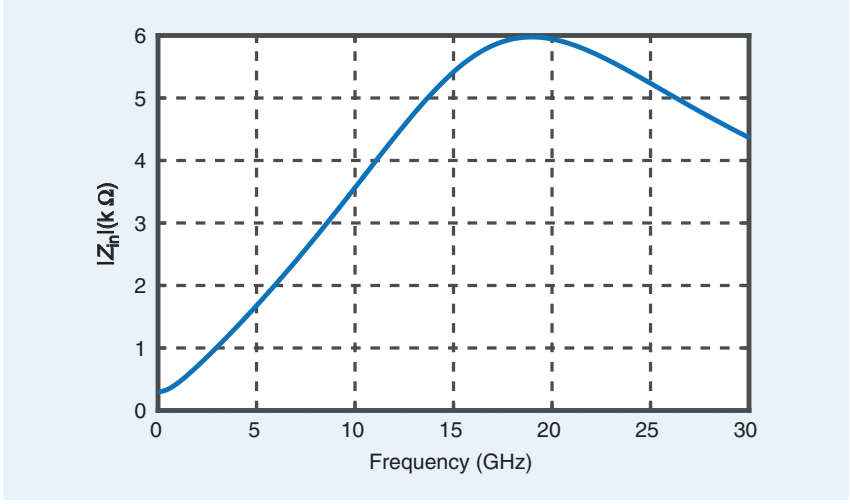

FIGURE 9: Simulated gyrator response.

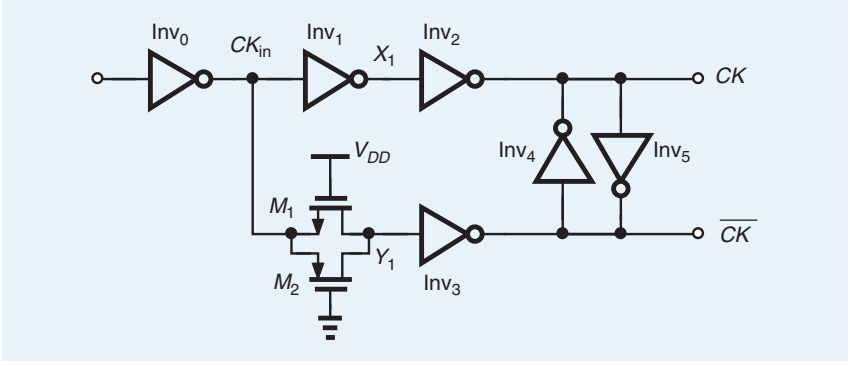

FIGURE 10: A single-ended to differential converter.

implying that a large equivalent inductance can be realized if G_{m1} and G_{m2} are small. However, the need for the negative sign complicates the design. With differential signals, we can envision the arrangement depicted in Figure 8(c), but the common-mode (CM) level at X and Y is highly sensitive to that of the input. As mentioned in the previous section, we can hang diode-connected inverters, Inv_5 and Inv_6, from these nodes so as to establish a suitable bias point. Unfortunately, the low impedance of these structures alters (7) to

$$Z_{in} = \frac{2C_1 s + G_{m5}}{G_{m1} G_{m2}}. \tag{8}$$

Consequently, the inductor incurs a series resistance and hence a lower Q.

We can partially cancel the impedance of Inv_5 and Inv_6 by attaching a negative resistance to each node [Figure 8(d)] [5]. Inverters Inv_7 and Inv_8 create, between X and Y, a resistance equal to $-2/G_{m7,8}$, yielding

$$Z_{in} = \frac{2C_1 s + G_{m5} - G_{m7,8}/2}{G_{m1} G_{m2}}. \tag{9}$$

Of course, if $G_{m7,8}/2$ is excessively close to G_{m5}, positive feedback caused by Inv_7 and Inv_8 may lead to latchup in an extreme corner of the process.

We simulate the circuit of Figure 8(d) with $(W/L)_P = 2(W/L)_N = 2\ \mu$m/30 nm for $Inv_1, \ldots, Inv_4$, $(W/L)_P = 2(W/L)_N = 1\ \mu$m/30 nm for Inv_5 and Inv_6, and $(W/L)_P = 2(W/L)_N = 0.5\ \mu$m/30 nm for Inv_7 and Inv_8. We also select $C_1 = 100$ fF. Plotted in Figure 9, the differential input impedance maintains a slope of 380 nΩ/Hz up to 15 GHz. Writing $Z = L_{eq}\omega$, we obtain $L_{eq} \approx 60$ nH. The gyrator consumes 0.8 mW.

The Single-Ended to Differential Converter

Many circuits, such as flipflops and comparators, operate with complementary clocks. In some cases, only one phase of the clock, CK_{in}, is available, requiring a stage that converts CK_{in} to differential outputs, CK and $\overline{CK}$.

Shown in Figure 10 is a structure that serves this purpose. The

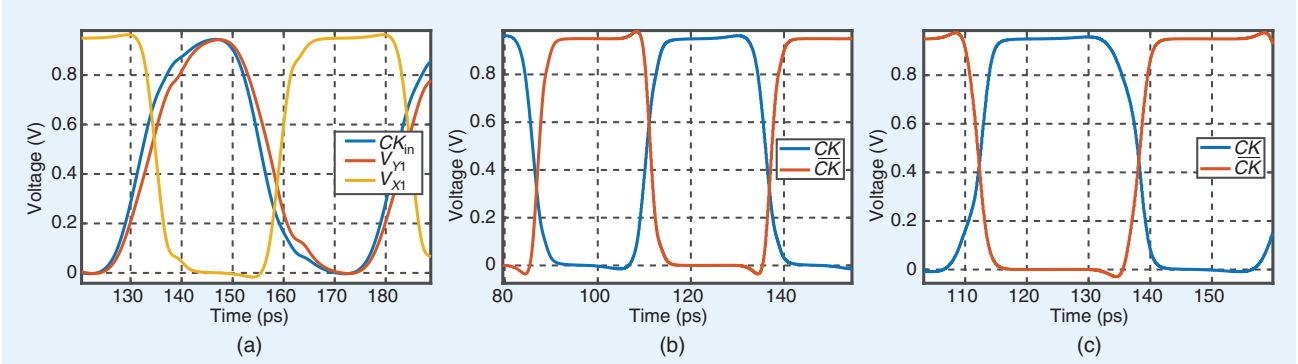

FIGURE 11: (a) Waveforms at X_1 and X_2, (b) waveforms at CK and $\overline{CK}$ without the cross-coupled inverters, and (c) waveforms at CK and $\overline{CK}$ with the cross-coupled inverters.

transmission gate (T-gate) consisting of M_1 and M_2 emulates the delay of Inv_1 without inversion, but X_1 and Y_1 are not quite complementary. This is for two reasons: 1) Inv_1 provides voltage gain, sharpening the transitions at X_1 while the T-gate does not, and 2) a falling edge at CK_{in} turns on the PMOS device in Inv_1 but propagates through both M_1 and M_2, experiencing less delay in the latter path. As a result, the waveforms at X_1 and Y_1 suffer from phase misalignment and duty cycle distortion, both undesirable at high speeds.

To alleviate these issues, we can adjust the N/P ratio. For example, with $(W/L)_N = (W/L)_P = 1\ \mu\text{m}/30\ \text{nm}$ for both Inv_1 and the T-gate, we obtain the waveforms plotted in Figure 11(a), where the inverting and noninverting paths still exhibit unequal delays, 2.9 ps and 1.7 ps, respectively. Without the cross-coupled inverters, the outputs appear as in Figure 11(b). We observe that CK and $\overline{CK}$ cross at a voltage higher or lower than $V_{DD}/2$.

We now add Inv_4 and Inv_5, with $(W/L)_N = (W/L)_P = 0.5\ \mu\text{m}/30\ \text{nm}$. As, for example, CK begins to fall, Inv_5 helps $\overline{CK}$ rise. Thus, the crossing points shift toward $V_{DD}/2$. Plotted in Figure 11(c) for a 20-GHz clock, the outputs are now nearly differential. The circuit draws 0.3 mW.

The Phase Alignment Circuit

Differential clock or data waveforms traveling through long interconnects may experience phase misalignment (skew) due to deterministic or random mismatches. The cross-coupled pair used in the previous section can correct only small skews.

We surmise that two clock phases, CK_{in} and $\overline{CK_{in}}$, can be aligned if a fraction of each is injected into the path of the other. Consider the topology presented in Figure 12, where without input misalignment, X_1 and Y_2 carry approximately the same waveform. T-gate TG_1 acts as an "equalizing" path between these nodes, pulling the waveforms toward each other in the presence of an input skew. Similarly, TG_2 equalizes Y_1 and X_2 [6].

We simulate the circuit for an input frequency of 20 GHz and with $(W/L)_P = 2(W/L)_N = 1\ \mu\text{m}/30\ \text{nm}$ for all of the stages. Illustrated in Figure 13(a) are the waveforms for a 20° input skew if TG_1 and TG_2 are absent. We observe that the skew, in fact, grows to $3.7\ \text{ps} \equiv 27°$ as it reaches CK and $\overline{CK}$. With TG_1 and TG_2 added, on the other hand, the results depicted in Figure 13(b) indicate a ten-fold reduction in the skew. The circuit consumes 0.35 mW.

The Low-Noise Amplifier

We have seen in this article series that a self-biased inverter can serve as a low-noise amplifier (LNA) in RF receivers. In modern direct-conversion systems, however, the circuit faces an issue. Consider the cascade shown in Figure 14(a), noting that today's mixers are designed as passive, current-mode topologies preceded by a transconductance stage and followed by transimpedance amplifiers (TIAs) so as to maintain small voltage swings and achieve high linearity. As a result, R_{mix} is typically no more than 100 Ω, severely reducing the voltage gain of the LNA. Thus, R_{LNA}, is no longer equal to the LNA's inverse transconductance. In the limit, $R_{mix} \to 0$ and $R_{LNA} \to R_F$, a value much higher than 50 Ω.

We can resolve this difficulty by means of "active" feedback, as illustrated in Figure 14(b) [7]. Denoting the voltage gain of Inv_1 by A_1 and the transconductances of Inv_2 and Inv_3 by G_{m2} and G_{m3}, respectively, we have

$$R_{LNA} = \frac{1}{A_1 G_{m2} R_{mix} G_{m3}} \qquad (10)$$

which can be set to 50 Ω. For example, if $G_{m2}R_{mix} \approx 1$ and $A_1 \approx 5$, we

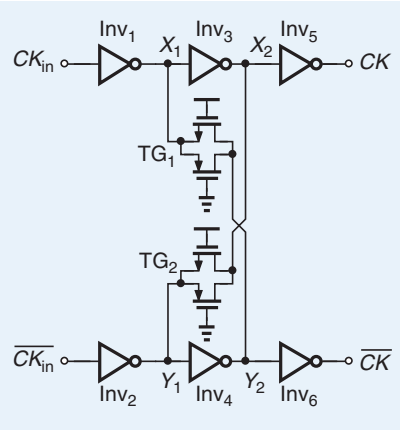

FIGURE 12: A phase alignment circuit.

select $G_{m3} \approx 1/(250\ \Omega)$, a reasonable value. The LNA's noise figure is derived in [7].

We simulate the LNA with $(W/L)_P = 2(W/L)_N = 16\ \mu$m/30 nm for Inv_1 and Inv_2 and $(W/L)_P = 2(W/L)_N = 2\ \mu$m/30 nm for Inv_3. We also assume $R_{\text{mix}} = 100\,\Omega$. Plotted in Figure 15(a) and (b) are the real and imaginary parts of the LNA's input impedance, revealing good matching across a wide bandwidth. The latter exhibits an inductive behavior because the loop gain falls as the frequency rises. Figure 15(c) reveals that $|S_{11}| < -10$ dB up to 8.5 GHz. Shown in Figure 15(d), the noise figure is less than 1 dB above 1 GHz and climbs at lower frequencies due to flicker noise.

Differential clock or data waveforms traveling through long interconnects may experience phase misalignment (skew) due to deterministic or random mismatches.

The Comparator With Programmable Threshold

In flash ADCs, a number of comparators compare the analog input to equally spaced voltages generated by a resistor ladder [Figure 16(a)]. Since the ladder can consume substantial power, it is desirable to employ comparators that rely on programmable "built-in" thresholds [Figure 16(b)]. Illustrated in Figure 16(c) is one implementation of this concept [8].

Resistive generation of the NMOS (PMOS) device shifts the inverter's input–output characteristic to the right (to the left). To the first order, equal increments in each resistor yield equal shifts in the inverter's trip point [Figure 16(d)].

The structure of Figure 16(c) entails two issues. First, equal increments in R_1 and R_2 do not actually lead to equal and opposite shifts unless M_1 and M_2 have the same strength and the same threshold voltage. Second, mismatches among inverters' trip points in a flash environment translate to offsets, producing differential and integral

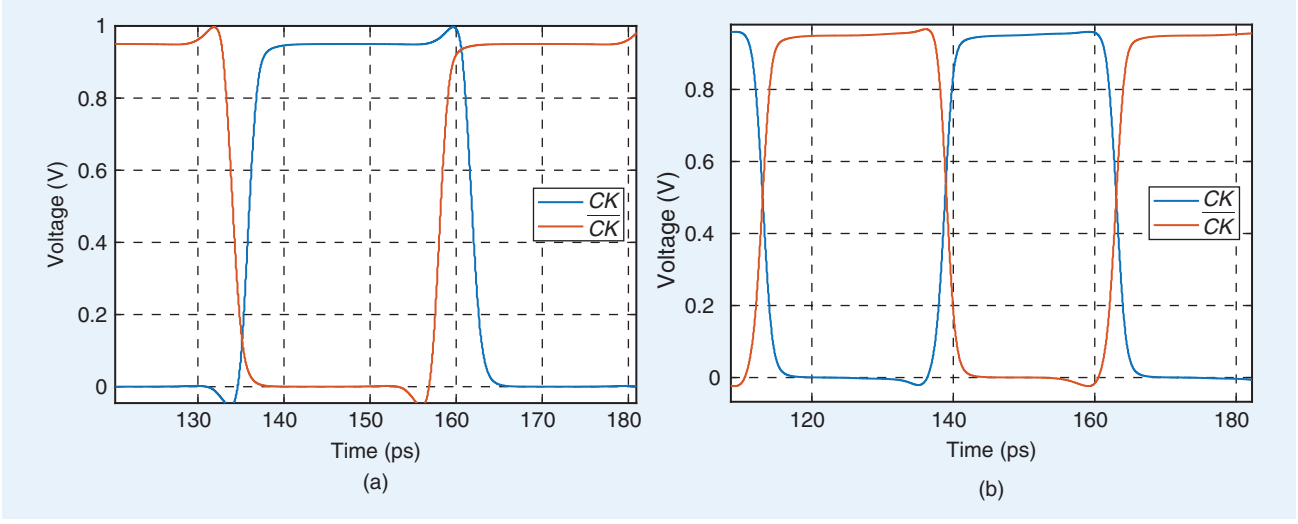

FIGURE 13: Simulated waveforms (a) before and (b) after adding T-gates.

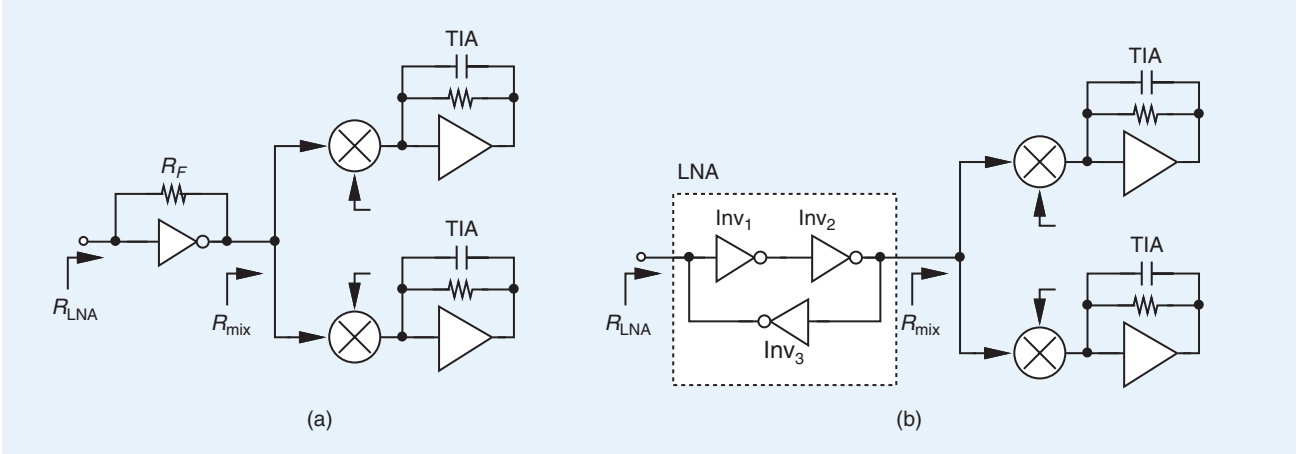

FIGURE 14: (a) Simple LNA followed by current-mode mixers and (b) LNA with active feedback followed by current-mode mixers.

nonlinearity. Some means of offset cancelation is therefore necessary.

We simulate the circuit of Figure 16(c) with $(W/L)_P = 2(W/L)_N = 2\ \mu m/30$ nm and $R_u = 200\,\Omega$. Plotted in Figure 17 are the resulting characteristics, exhibiting negative shifts equal to 10.5 mV and 9.3 mV and positive shifts equal to 7.2 mV and 6.4 mV. The latter two correspond to degeneration of M_1 and depart significantly from the former two. More uniform shifts thus require fine tuning of the transistors' dimensions.

The Class-D Amplifier

Shown in Figure 18(a), a class-D stage delivers nearly rail-to-rail, differential voltage swings to a load, R_L. Also called an *H-bridge* and naturally formed by two CMOS inverters, this topology achieves

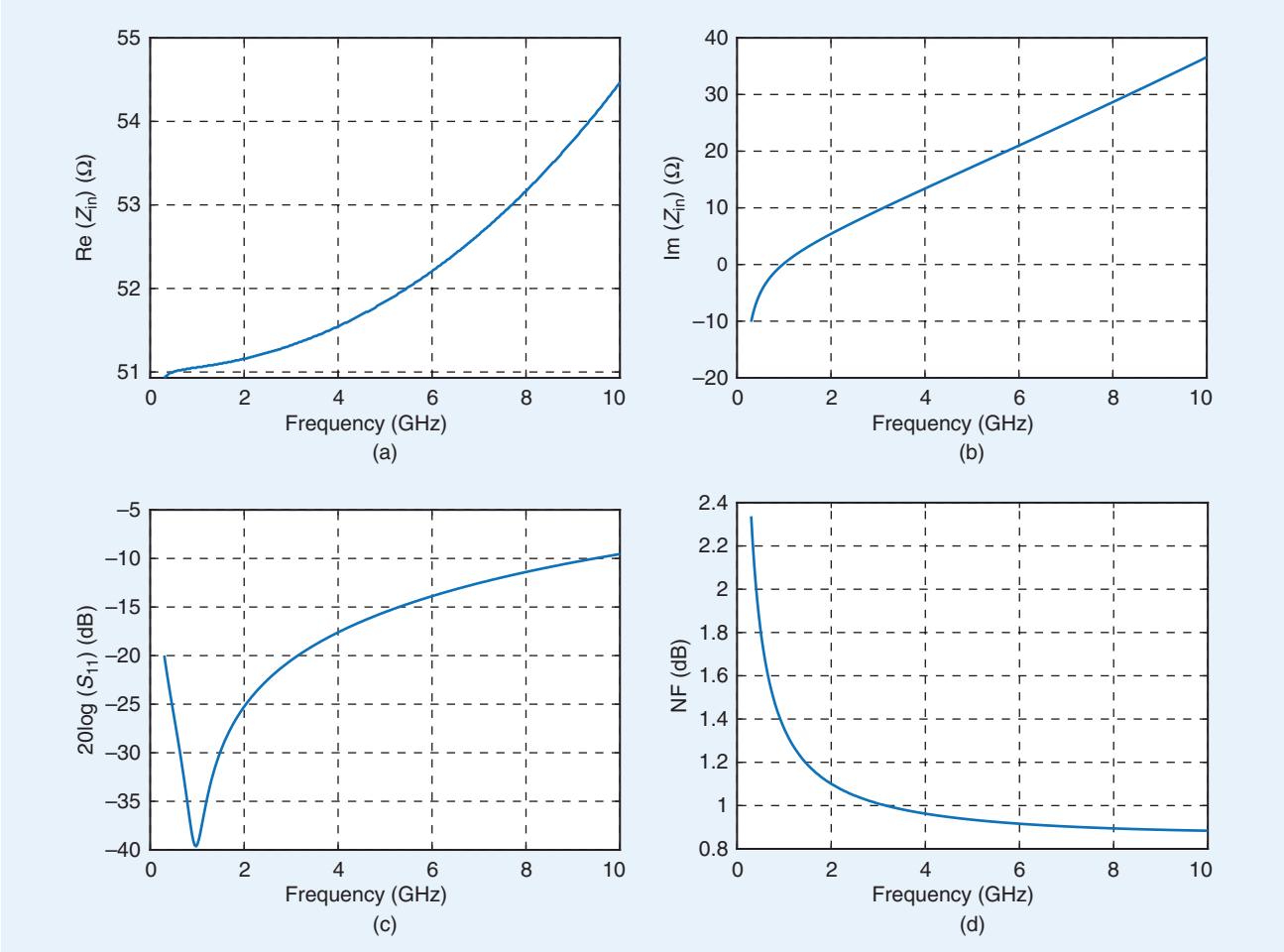

FIGURE 15: (a) Real part of LNA input impedance, (b) imaginary part of LNA input impedance, (c) S_{11}, and (d) NF.

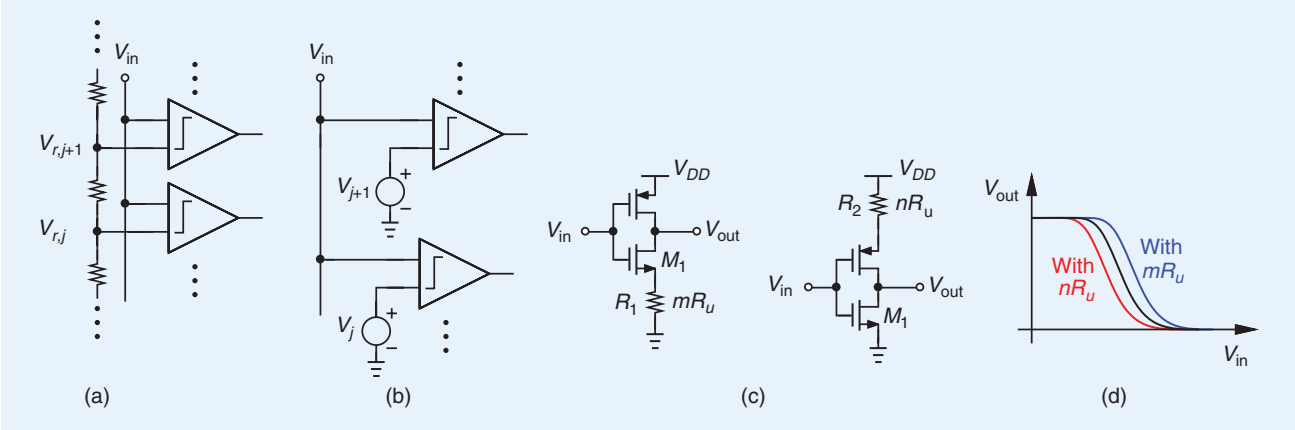

FIGURE 16: (a) Simple flash ADC, (b) concept of comparators with built-in offset, and (c) possible realization of the idea.

a high power efficiency if the on-resistance of the switches is minimized, but it operates only with a digital signal, D_{in}. Fortunately, the circuit can also be used in analog systems.

Suppose we wish to deliver an analog signal to a low load resistance, e.g., an 8-Ω speaker. This proves particularly challenging in high-quality music applications, where the distortion must remain below −100 dB. Highly linear "analog" amplifiers suffer from a low power efficiency.

We instead envision that a digital waveform swinging between zero and V_{DD} and carrying the desired signal can yield a higher efficiency if its undesired frequency components are filtered before reaching the load. The digital waveform is typically a pulsewidth-modulated (PWM) signal and the amplifier is realized as a class-D configuration. Illustrated in Figure 18(b), the overall circuit consists of a triangular-wave generator running at a frequency of f_{tr}, an unclocked comparator, $Comp_1$, a class-D stage, and output LC filters. $Comp_1$ is implemented by a high-gain amplifier that produces a high (low) level when V_{in} slightly exceeds (falls below) V_{tr}. The output is thus a PWM signal whose spectrum contains that of V_{in} along with those in the vicinity of f_{tr}. We then apply V_{PWM} to buffers and a class-D stage to drive the load.

Our class-D amplifier delivers 35 mW of power while drawing 45 mW, providing an efficiency of 77%.

We should make two remarks. First, for a high efficiency, the transistors comprising Inv_1 and Inv_2 in Figure 18(b) must be wide enough to provide an on-resistance much less than 8 Ω/2, e.g., a value in the range of a few tens of milliohms. Second, for audio applications, the low-pass filters require high capacitance and inductance values and are placed off-chip.

We simulate the circuit with a 20-kHz input sinusoid and a 2-MHz triangular waveform. The comparator is realized by a two-stage op amp and, for Inv_1 and Inv_2, we select $(W/L)_P$=2$(W/L)_N$=900 μm/30 nm. Also, $L_1 = L_2 = 10$ μ H and $C_1 = C_2 = 100$ nF. In Figure 19(a), we observe the input waveform along with the comparator PWM output, noting that the latter remains high or low most of the time at the peaks of the former. That is, the average value of V_{PWM} tracks V_{in}.

Displayed in Figure 19(b) are the differential voltages reaching $R_L = 8\,\Omega$, exhibiting a peak-to-peak swing of 750 mV. Figure 19(c) plots the output spectrum and reveals a third harmonic 64 dB below the fundamental. In high-quality audio systems, the circuit is placed in a negative-feedback system to reduce the distortion.

Our class-D amplifier delivers 35 mW of power while drawing 45 mW, providing an efficiency of 77%. In practice, efficiencies near 99% are sought by ensuring that Inv_1

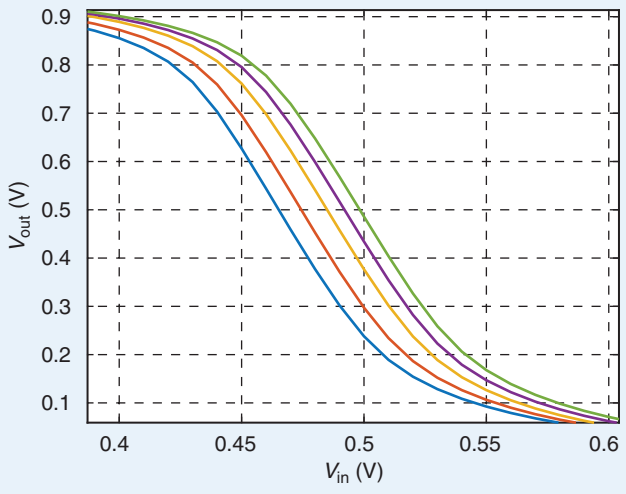

FIGURE 17: Simulated characteristics of degenerated inverters.

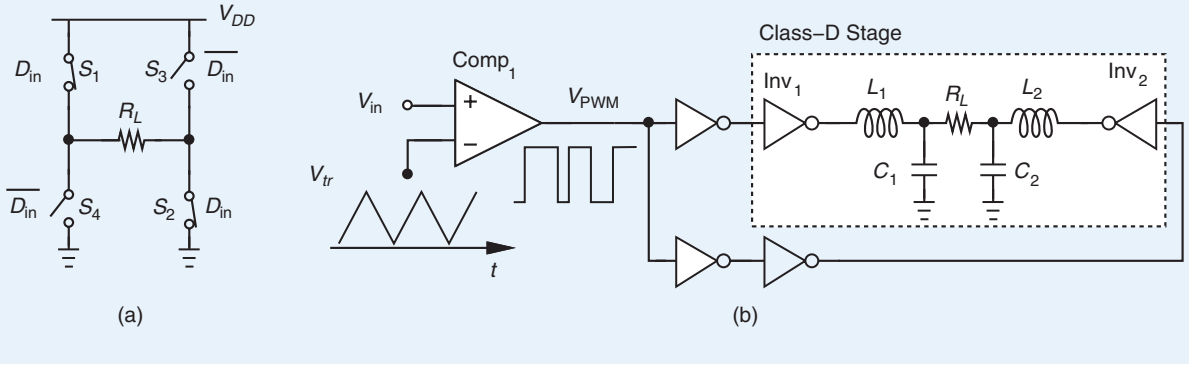

FIGURE 18: (a) A simple class-D stage and (b) class-D amplifier with PWM input.

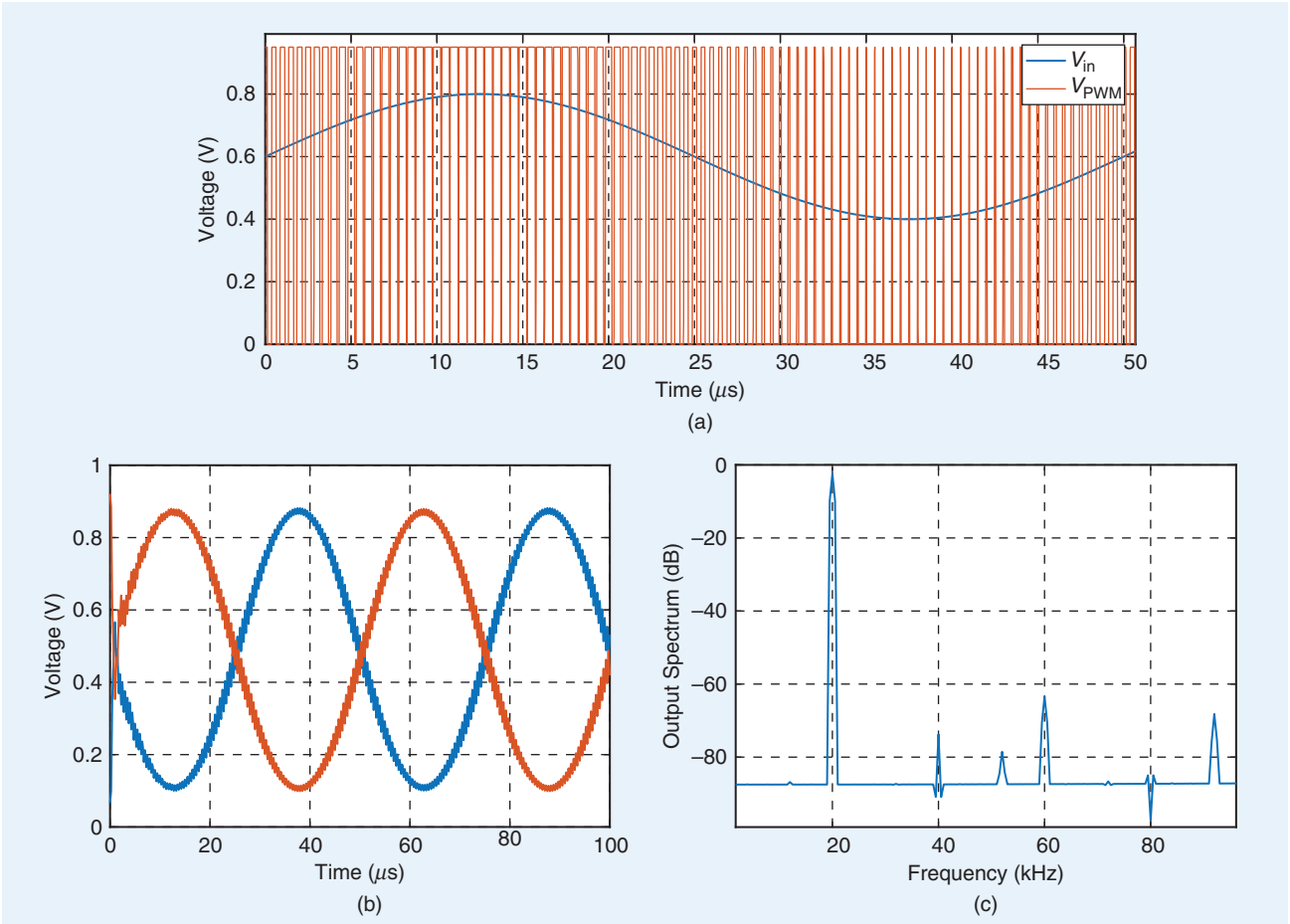

FIGURE 19: (a) Input and comparator output waveforms, (b) load voltage waveforms, and (c) output spectrum.

and Inv_2 incur minimal crowbar currents (flowing directly from V_{DD} to ground).

The Linearized Transconductor

Transconductance stages, also known as "transconductors," are widely used in analog filters. Processing a large desired signal and possibly an even larger undesired component, such filters must exhibit sufficient linearity to avoid distortion, compression, and intermodulation.

A single inverter can serve as a transconductor if its transistors remain in saturation, but with poor linearity. Consider the arrangement shown in Figure 20(a), where the output current is monitored as V_{in} ranges from zero to V_{DD}. The derivative of I_{out} with respect to V_{in} yields the G_m behavior plotted in Figure 20(b). We recognize that, for a maximum nonlinearity (change in G_m) of, e.g., 0.2%, the input voltage range is confined to about 30 mV around 375 mV.

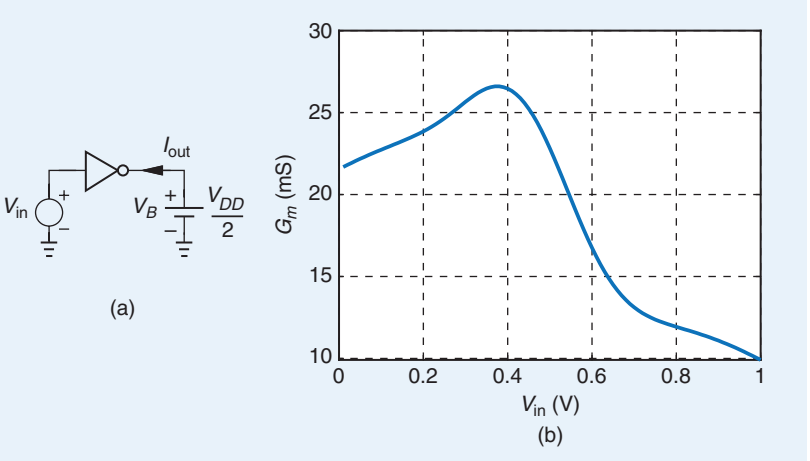

FIGURE 20: (a) An inverter acting as a transconductor and (b) its transconductance behavior.

To improve the linearity, we can place one copy of the inverter in a negative-feedback loop and use the result to drive another. Depicted in Figure 21 [9], the circuit incorporates amplifier A_1 and Inv_1 to establish a virtual ground at X. It follows that Inv_1 must absorb a small-signal current equal to V_{in}/R_1, causing the

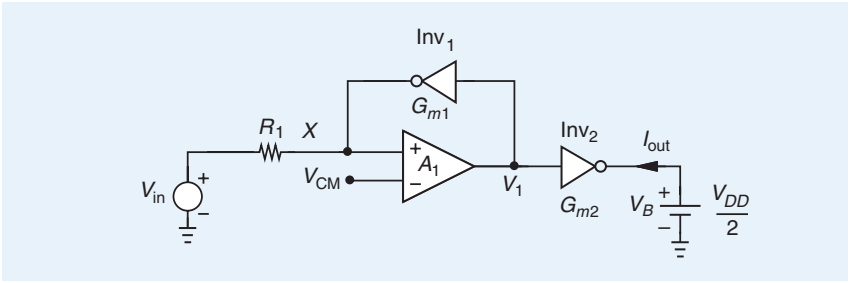

FIGURE 21: Linearized transconductors.

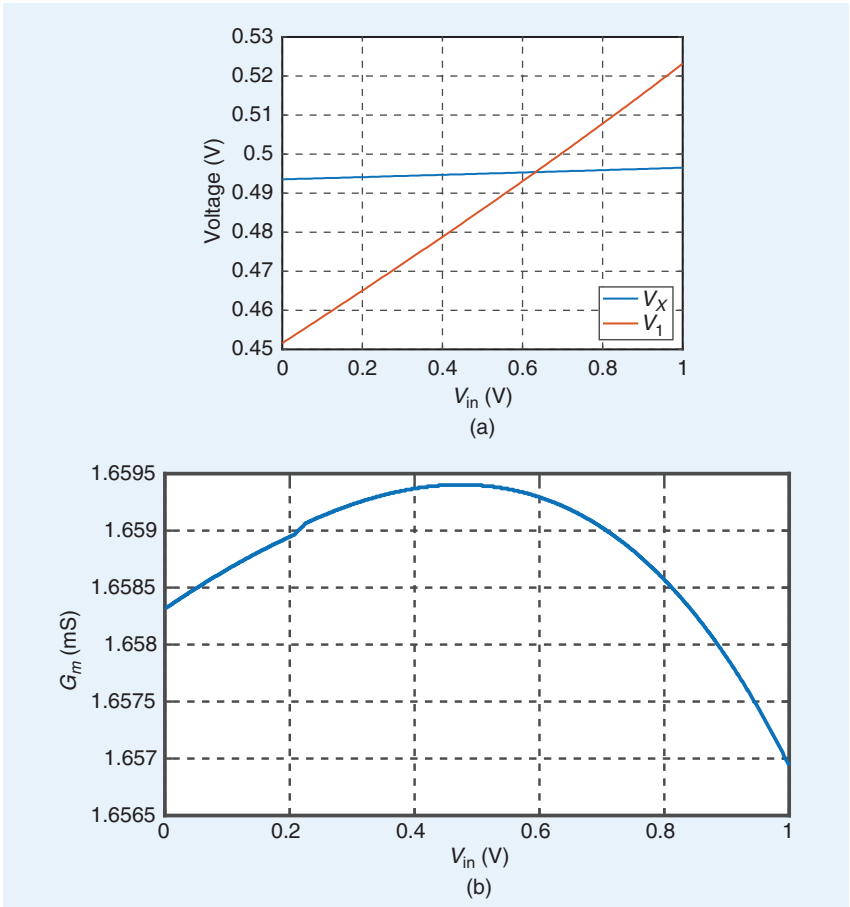

FIGURE 22: (a) V_X and V_1 as a function of V_{in} and (b) overall transconductance as a function of V_{in}.

loop to generate $V_1 = (V_{in}/R_1)/G_{m1}$. That is,

$$\frac{I_{out}}{V_{in}} = \frac{G_{m2}}{G_{m1}R_1}. \tag{11}$$

If Inv_2 is simply a scaled version of Inv_1, we have

$$\frac{I_{out}}{V_{in}} = \frac{\alpha}{R_1} \tag{12}$$

where α is the scaling factor. Two key points emerge here. First, the overall transconductance is fairly independent of G_{m1} and G_{m2}, displaying high linearity. Second, for this to occur, we must choose $G_{m1}R_1$ large enough so that V_1 has a small swing. Note that, without V_B, the output voltage range of Inv_1 is the same as that of Inv_2 and hence very narrow.

We simulate the circuit of Figure 21 with $(W/L)_P = 2(W/L)_N = 2\,\mu m/30\,nm$ for Inv_1 and eight times these values for Inv_2. Thus, $\alpha = 8$, which along with $R_1 = 5\,k\Omega$, should give an overall transconductance of about 1.6 mA/V. We implement A_1 as a five-transistor operational transconductance amplifier with $W/L = 25\ \mu m/120$ nm for all of the transistors and a tail current of 50 μA, obtaining $A_1 \approx 28$ dB.

Plotted in Figure 22(a) are V_X and V_1 as V_{in} varies from zero to V_{DD}. They change by only 3 mV and 72 mV, respectively. Figure 22(b) presents the transconductance, which is close to the predicted value of 1.6 mA/V, and has a peak-to-peak variation of 0.14%.

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