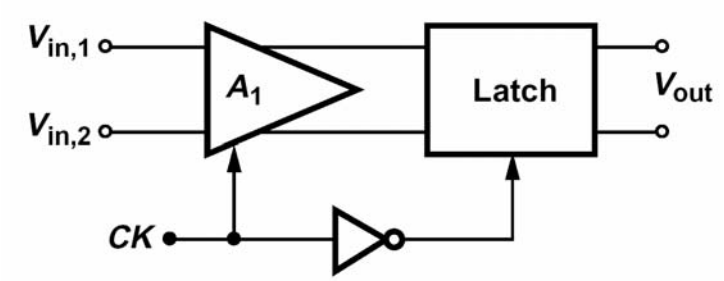
CMOS Comparators

Basic Concepts



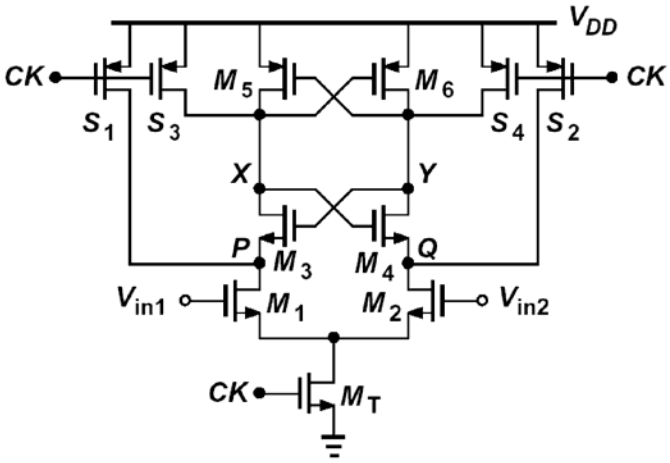
Need to provide high gain, but it doesn't have to be linear

- **Don't need negative feedback and hence don't have to worry about phase margin.**
- **The gain can be obtained in multiple stages.**

Important parameters:

Offset (and noise), speed, power dissipation, input capacitance, kickback noise, input CM range.

Example



(Wang & Razavi, JSSC, March '00)

Input Offset

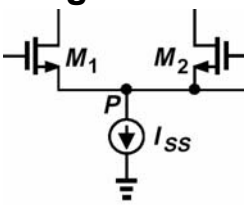
Offset originates from two circuits: the preamplifier and the latch:

$$\left(V_{os,tot}\right)^2 = \left(V_{os,pre}\right)^2 + \left(\frac{V_{os,latch}}{A_{pre}}\right)^2$$

Need to choose high A_{pre} to suppress the effect of $V_{os,latch}$.

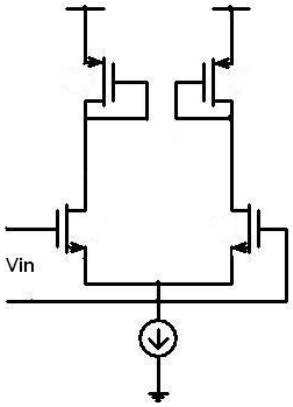
CMOS latches, especially with small devices, have large offsets.

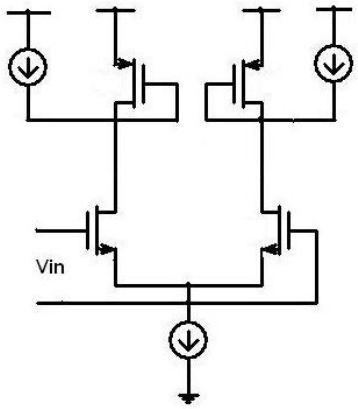
$$V_{OS} = \Delta V_{TH} + 2\left(\frac{\Delta W}{W} - \frac{\Delta L}{L}\right)(V_{GS} - V_{TH})$$



When the latch is strobed, the cross-coupled devices have a large VGS and hence large mismatch.

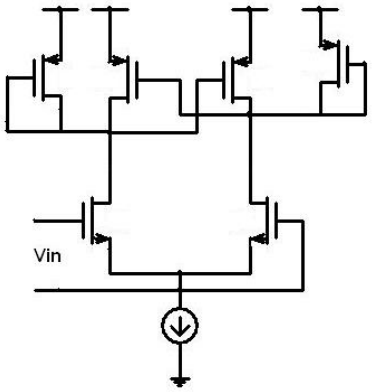
Preamplifier Topologies





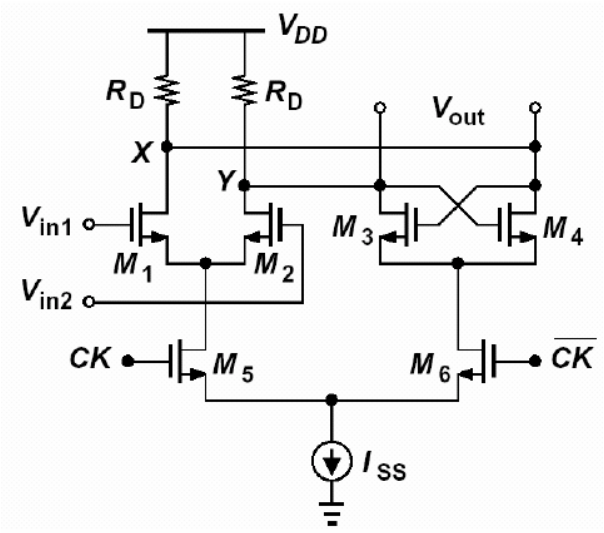
- Limited gain **- Trades gain with speed**

- Direct trade-off between gain and headroom.



- Positive feedback tends to slow down overdrive recovery.
- Gain is well-defined:

Current-Steering Topology:

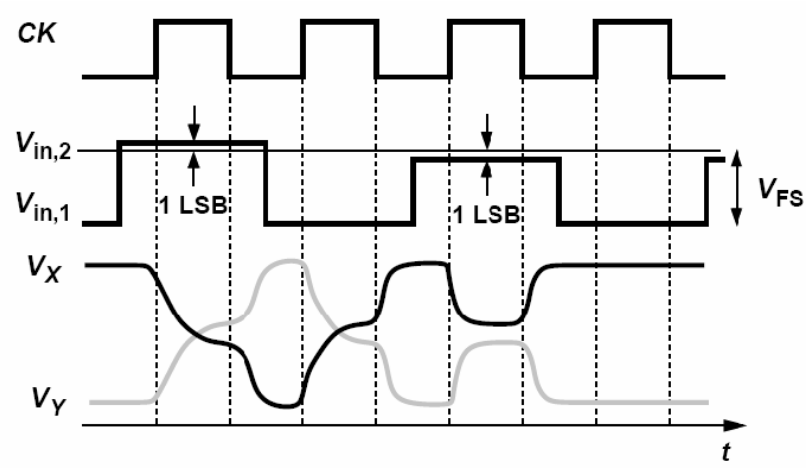


Speed

Two distinct speed limitations: preamplifier overdrive recovery, and latch regeneration speed. The former is usually the bottleneck.

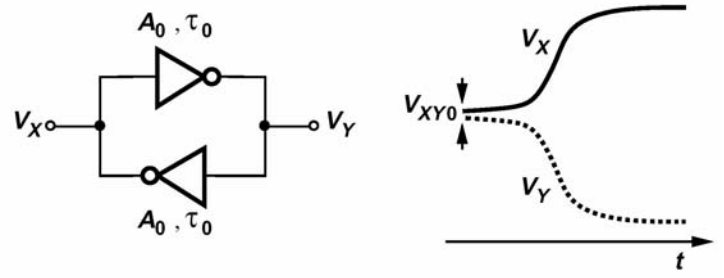
Tradeoffs between: gain, power dissipation and overdrive recovery speed.

Overdrive Test:



Metastability

Positive feedback provides infinite gain if given infinite time.

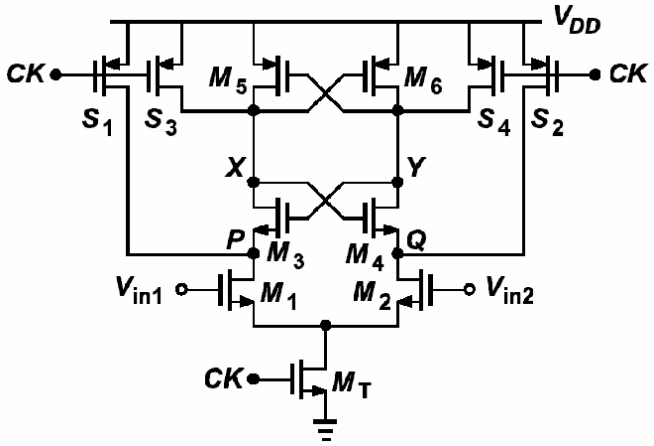


If input is uniformly distributed between $-V_{XY1}$ and $+V_{XY1}$, then the probability that output does not reach V_{XY1} within T_C seconds is:

$$P(T_1 > T_c) = \exp \frac{-(A_0 - 1)T_c}{\tau_0}$$

Kickback Noise

Switching operations inside a comparator can feed through capacitances back to the input:

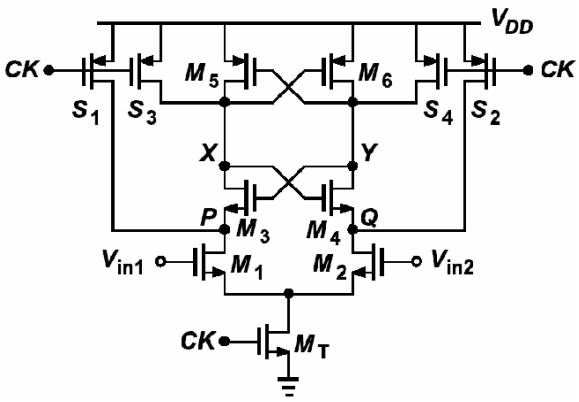


Input CM Range

In many cases, comparators must be able to handle a large common mode range. Since for a one-stage amplifier, we have a tradeoff between gain and voltage headroom, the input CM range is limited.

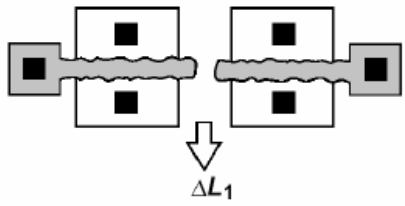
RS Latch

Comparators used in A/D converters are usually followed by an RS latch.

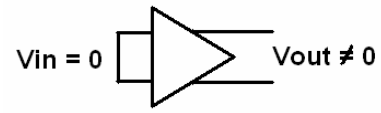


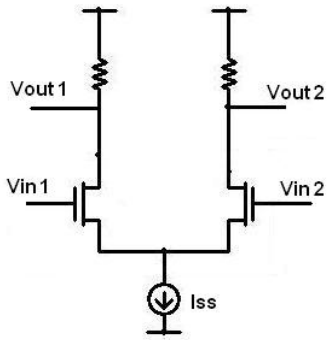
Mismatch Revisited

Random, microscopic variations during fabrication create mis-matches between nominally identical devices:



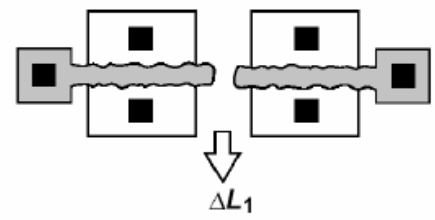
Mismatches manifest themselves as offsets (and finite CMRR) in amplifiers:

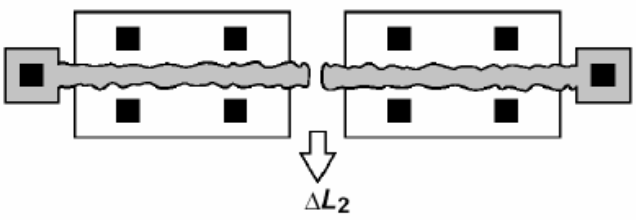




Observations

- Mismatches decrease with device area because more "averaging" is afforded. For example, increasing the device width improves the length mismatch as well:





MOS devices mismatch is typically considered for two parame-ters: thereshold voltage mismatch, ΔV_{TH}, and $\mu C_{ox}W/L$ mismatch.

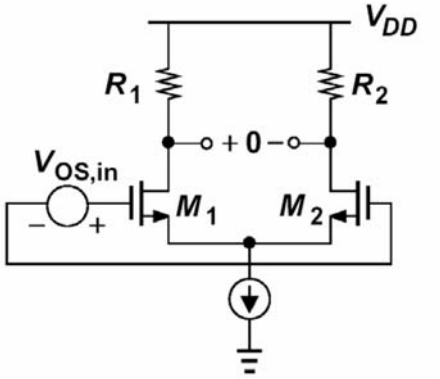
- It's been verified mathematically and experimentally that:

$$\Delta V_{TH} = \frac{A_{VTH}}{\sqrt{WL}}$$

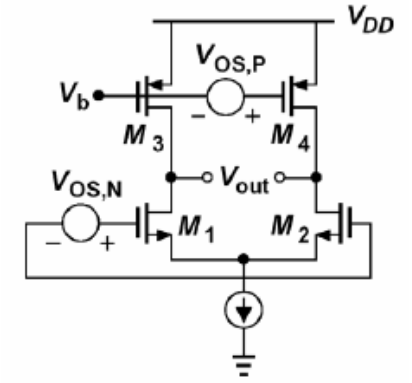
$$\Delta \mu C_{OX} \frac{W}{L} = \frac{A_k}{\sqrt{WL}}$$

- Offset is similar to noise: if the two inputs of a differential pair are shorted together, the output is nonzero and varies with time due to noise.

- Offset of a Differential Pair

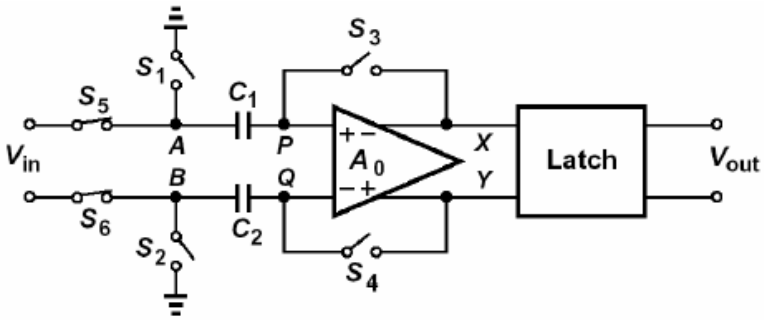


Example:



Offset Cancellation

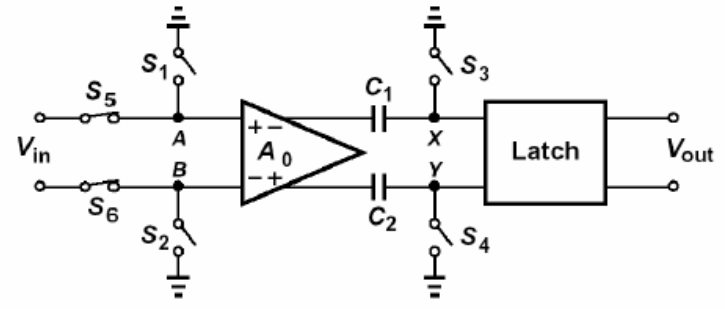
Input Offset Storage



$$V_{os,tot} = \frac{V_{osA}}{1 + A_o} + \frac{\Delta q}{C} + \frac{V_{osL}}{A_o}$$

- Rail-to-Rail CM Range
- Fast Recovery
- Large Input Cap
- A_o must be large

Output Offset Storage

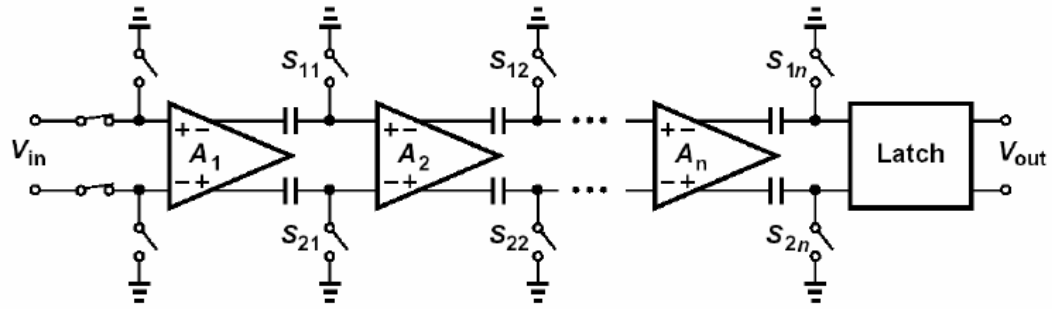


- Limited CM Range
- Slow Recovery
- Smaller Input Cap
- Lower Offset

Note: Gain of preamp cannot be very high here because $V_{OSA}.A_o$ may saturate the output.

The offset of latch may be dominant in both cases.

Multistage Offset Cancellation

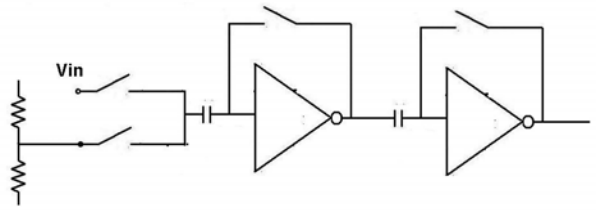


How much is the overall offset voltage?

- Complexity and power are generally quite high.

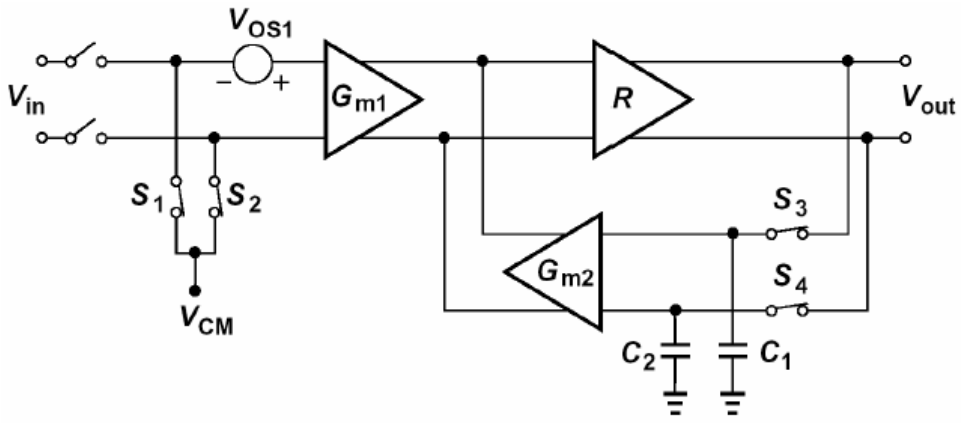
- Used only in high-precision systems, e.g. V_{OS} < 0.5 mV.

Don't try this at home:



Noninvasive Offset Cancellation

- Cancellation techniques described above introduce large parasitics in signal path (especially troublesome for op amps).



First, assume inputs of G_{m1} and G_{m2} are grounded.

V_{out} =

Now, if the $G_{m2}R$ loop is closed:

What happens if the switches have charge injection mismatch?

$$\frac{\Delta Q}{C} x G_{m2} R \bullet \frac{1}{G_{m1} R}$$

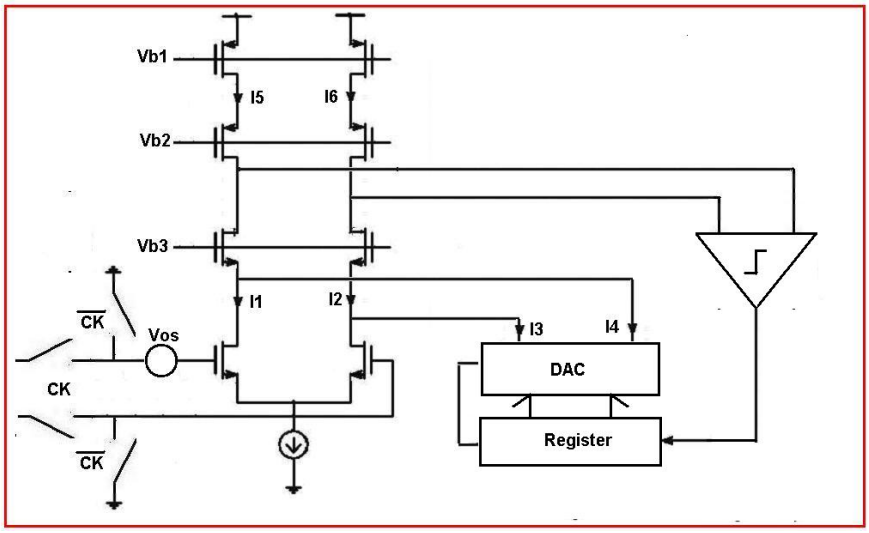
- **Total input-referred offset:**

$$V_{os,tot} = \frac{V_{os1}}{G_{m2}R} + \frac{V_{os2}}{G_{m1}R} + \frac{G_{m2}}{G_{m1}} \bullet \Delta V$$

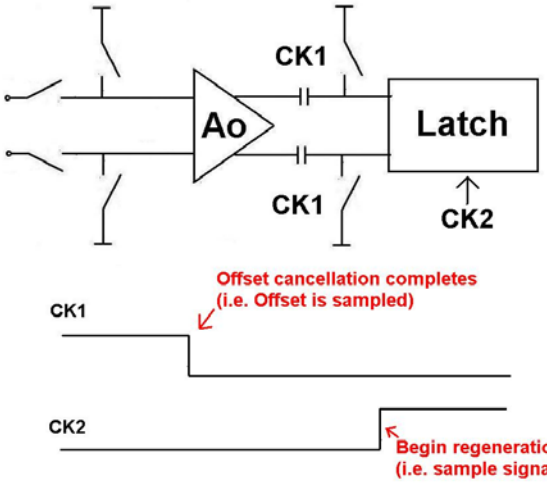
Implementation:

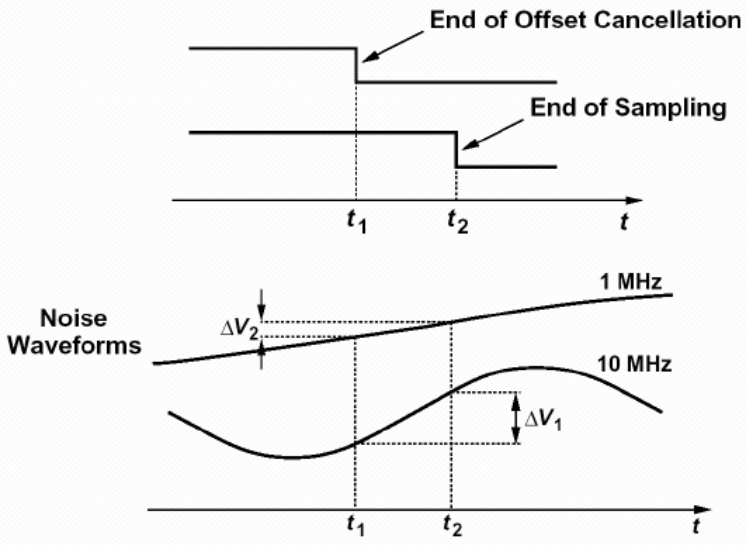
Note that Gm2 does not affect the signal path significantly. But input switches may. Only drawback is the need to periodically refresh (due to charge leakage).

Alternative solution is to store the offset digitally:



Correlated Double Sampling (CDS)





If amplitude of noise components after t1 is correlated (e.g., similar) with that before t1, the noise is also suppressed.
The effect is like a high-pass filter transfer function. Good for 1/f noise. (But wideband noise is aliased.)

Refer to ENZ & Temes, Proc. IEEE Nov. '96