

**Thermal Analysis of
Vertical-Cavity Surface-Emitting
LED/VCSEL Assembly with
Lead-Free Flip Chip Interconnects**

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Objectives

- ✍ To determine the effects of interconnect materials and ambient temperature on the steady-state temperature distribution of a 2x2 area array parallel vertical-cavity surface-emitting LED/VCSEL assembly.
- ✍ The light sources are deposited on a GaAs chip, which is mounted on a Si-substrate with four flip chip solder joints.
- ✍ Two kinds of solders, namely, 63Sn-37Pb and 80Au-20Sn, are studied.

Outline of Presentation

-  Introduction and Overview
-  Description of Assembly Configuration
-  Finite Element Modeling
-  Thermal Analysis and Discussion
-  Concluding Remarks

Introduction

Fiber-Optic Communication Systems

- * Light Sources
- * Optical Fibers
- * Optical Receivers



The electrical signal is converted into the optical signal through the *light source*.

The optical signal is transmitted through the *optical fiber*.

The optical signal is converted back into the electrical signal through the *optical receiver*.

Light Sources

Most of the light sources are based on the electron-hole recombination in semiconductor materials. This recombination results in the release of energy (in the form of another photon), which can take place:

-  **SPONTANEOUSLY** such as the light-emitting diodes (LEDs), which are used for very short distance such as chip-to-chip communications with plastic fibers.
-  **As a result of an EXTERNAL STIMULUS** such as the semiconductor lasers, which are used for long distance telecommunications.

For both LEDs and semiconductor lasers, they can collect the light in the direction parallel to the p-n junction and are called the edge-emitting diodes and edge-emitting lasers, respectively.

They can also collect the light in the direction perpendicular to the p-n junction and are called the surface-emitting diodes and vertical-cavity surface-emitting lasers (VCSELs), respectively.

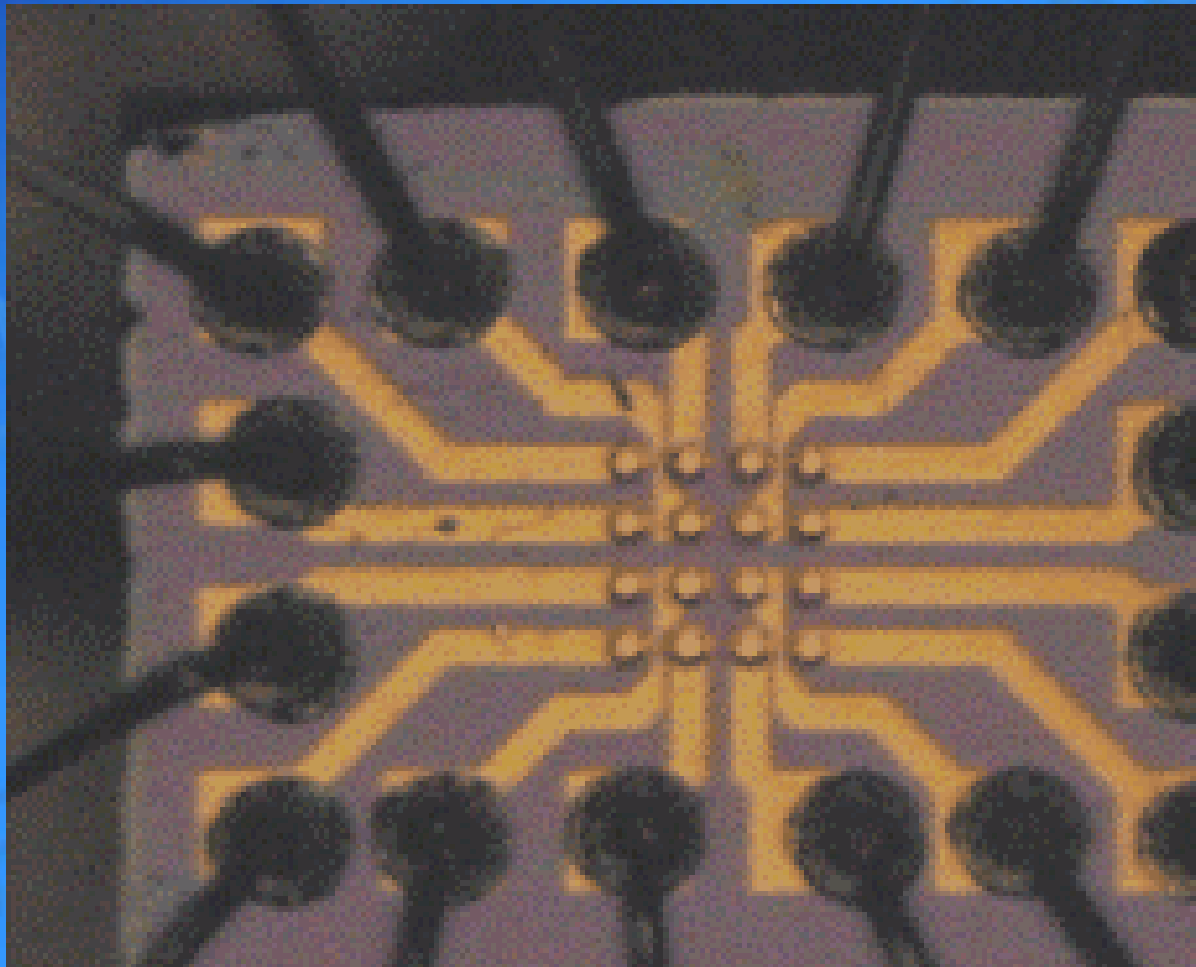
One of the advantages of surface-emitting light sources is that they can be used in parallel optics that offer low-cost interconnection with perhaps the best use of backplane space in a network system.

In principle, the wavelength in the infrared region has the advantage of integrating large 2-D emitter arrays with active (such as CMOS driver) components. This is because the semiconductor becomes transparent in this wavelength region and, therefore, the device can emit lights through the substrate.

This feature yields to the possibility of applying the conventional flip chip technology to the LED/VCSEL assembly.

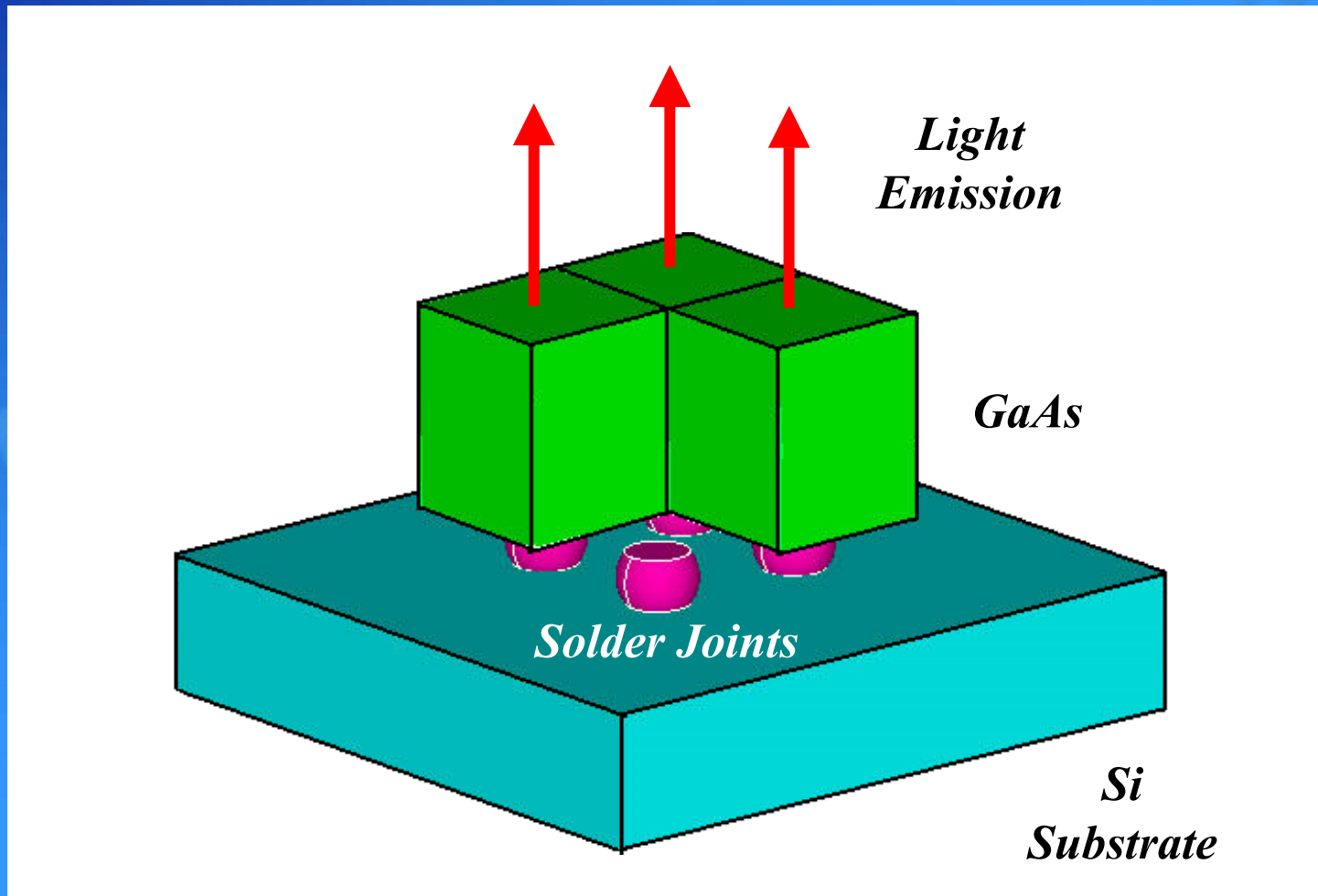
One of the major advantages of solder-bumped flip chip technology is the self-alignment capability.

4x4 VCSEL Array with 16 Wire Bonds



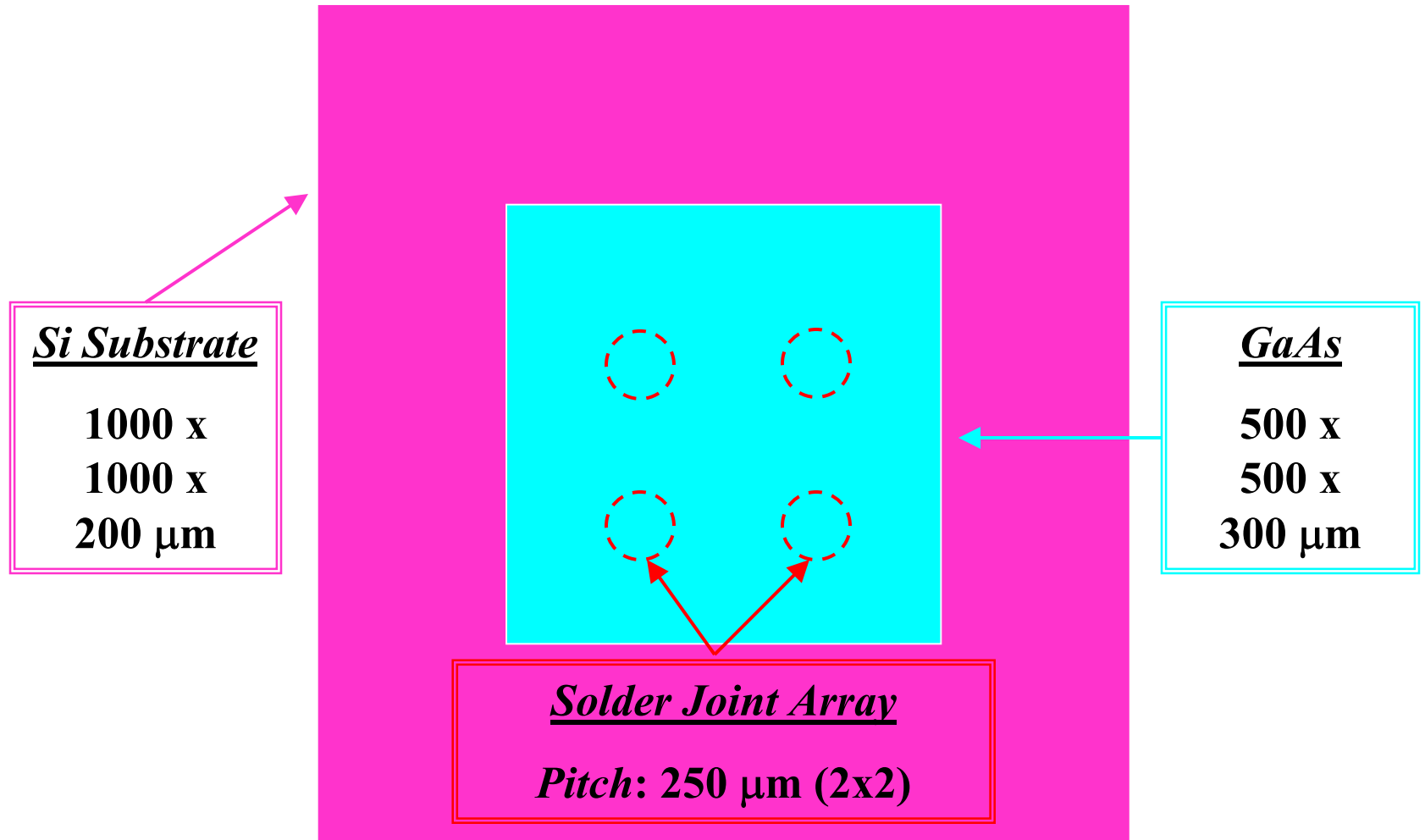
Courtesy of Honeywell

Configuration of VCSEL Assembly

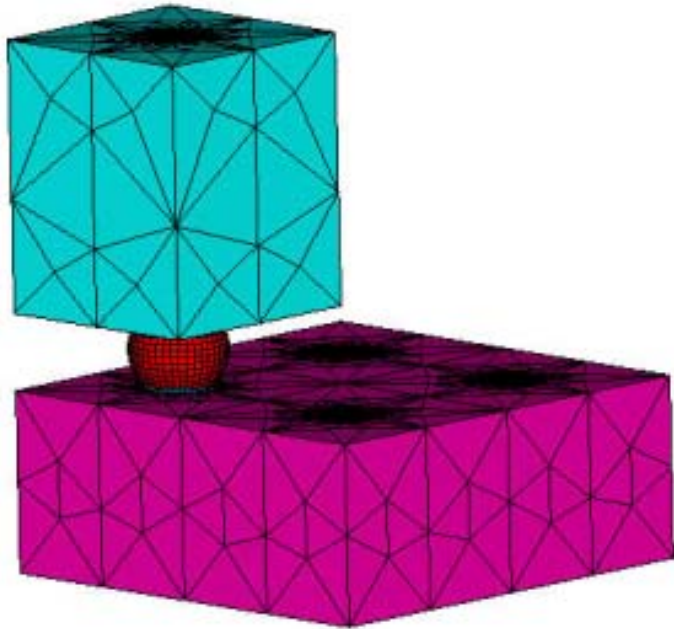


(A quarter of the GaAs chip is removed to observe the solder joints)

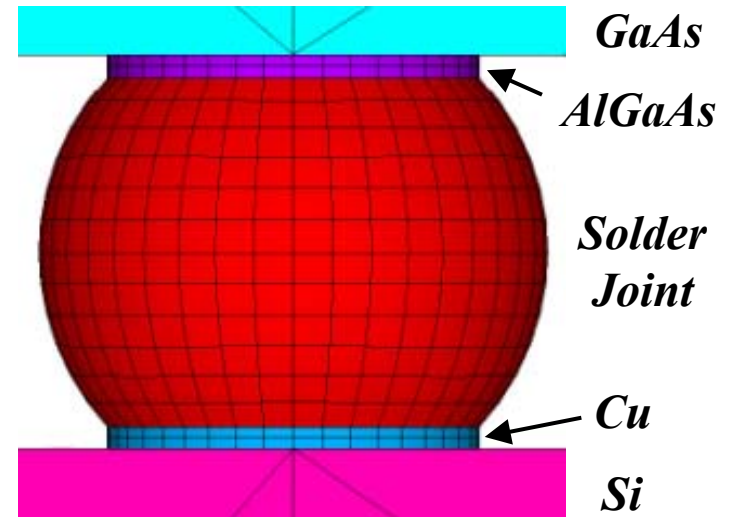
Dimensions of VCSEL Assembly



Finite Element Meshes



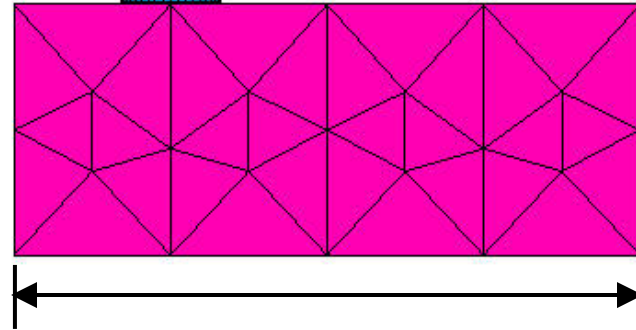
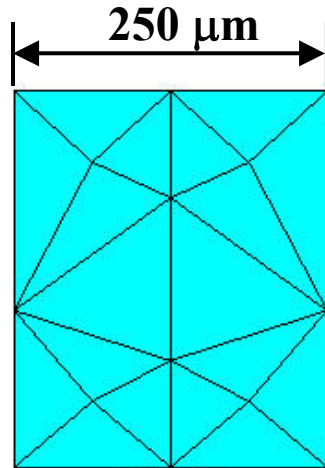
Finite Element Mesh of a Quarter Whole VCSEL Assembly



Local Finite Element Mesh of AlGaAs/Solder Joint/Cu Pad

Dimensions of Finite Element Model

(Thickness: 300 μm)



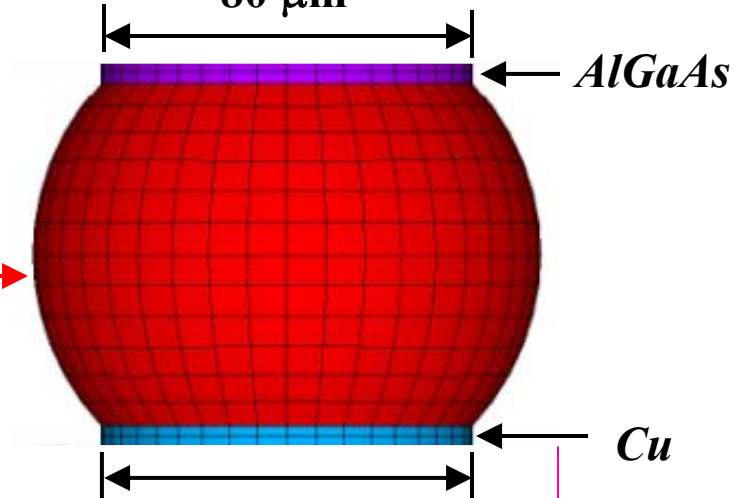
500 μm
(Thickness: 200 μm)

Solder Bump Size:
100 μm

Bump Height:
75 μm

(Thickness: 5 μm)

80 μm



Cu

80 μm
(Thickness: 5 μm)



Finite Element Thermal Analysis

ANSYS V. 5.7

SOLID70 3-D 8-node Element

Steady-State Thermal Conduction

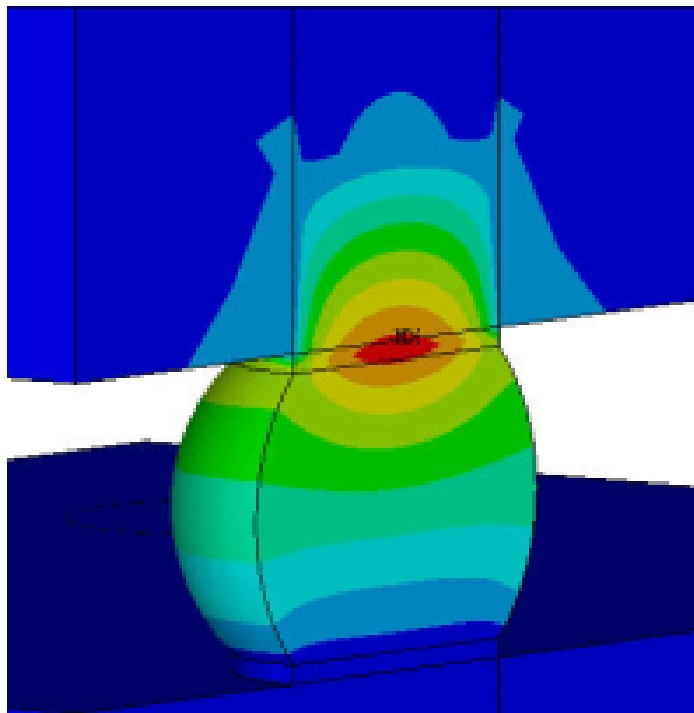
Heat Source: AlGaAs (1 mW)

Ambient Temperature: 27°C or 55°C

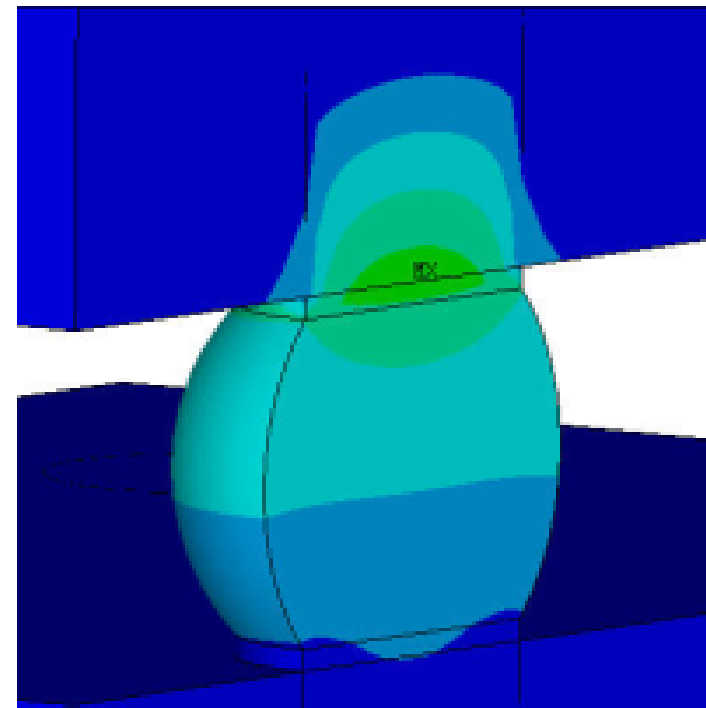
Thermal Conductivity for Modeling

Materials	Thermal Conductivity (W/m•K)
GaAs	33.7
AlGaAs	33.67
63Sn-37Pb	50.6
80Au-20Sn	251
Cu	400
Si	165

Temperature Contours (I)



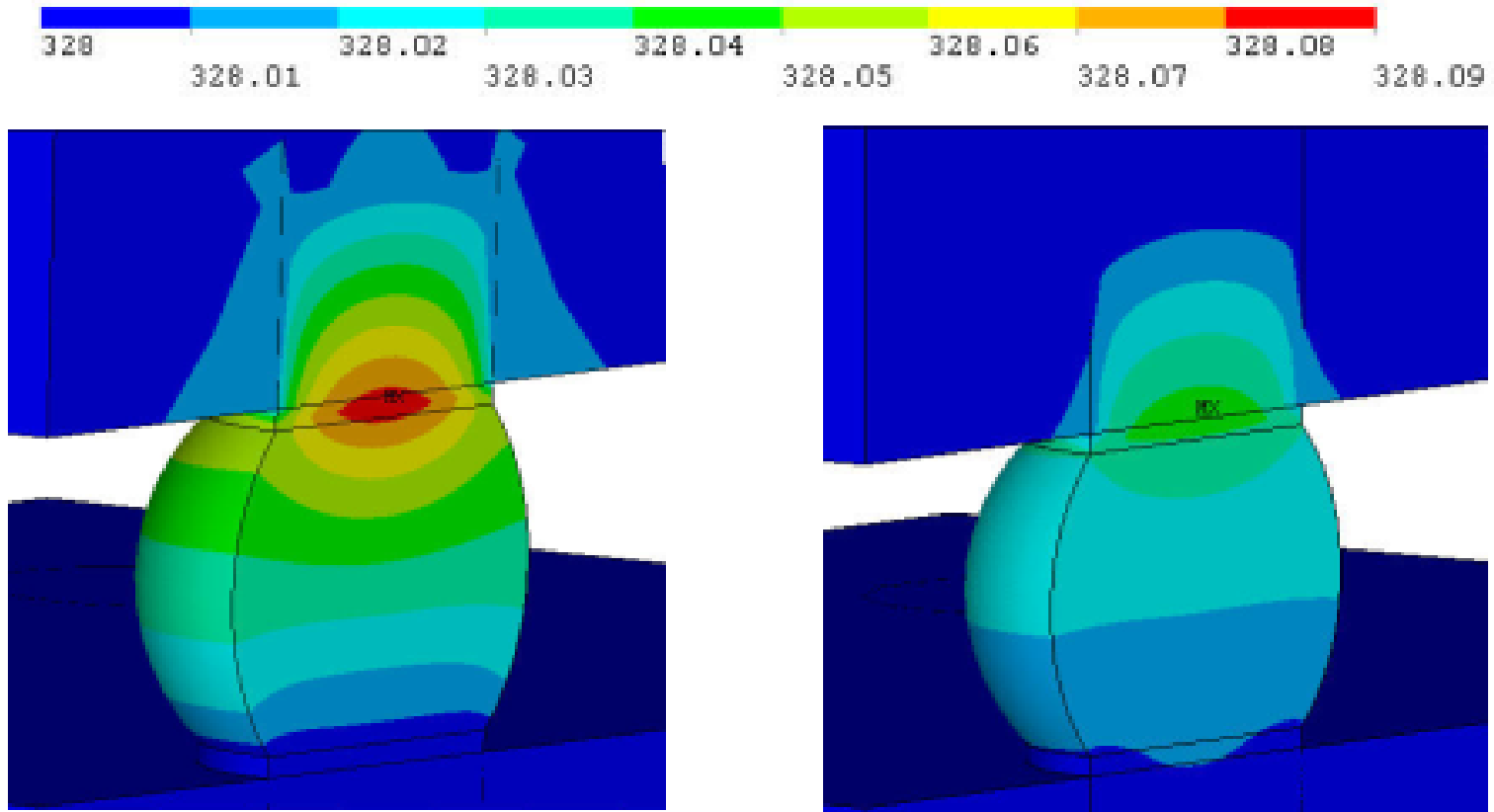
63Sn-37Pb



80Au-20Sn

Ambient Temperature = 27°C

Temperature Contours (II)



$63\text{Sn}-37\text{Pb}$

$80\text{Au}-20\text{Sn}$

Ambient Temperature = 55°C

Consideration of Heat Convection

Heat-Transfer Coefficients

Ambient Temperature = 25°C

The back of the GaAs Chip = $1.017 \times 10^{-5} \text{ W/}^\circ\text{C-mm}^2$

The side of the GaAs Chip = $2.662 \times 10^{-5} \text{ W/}^\circ\text{C-mm}^2$

The top of the GaAs Chip = $2.662 \times 10^{-5} \text{ W/}^\circ\text{C-mm}^2$

The back of the Si Chip = $2.163 \times 10^{-5} \text{ W/}^\circ\text{C-mm}^2$

The side of the Si Chip = $2.662 \times 10^{-5} \text{ W/}^\circ\text{C-mm}^2$

The top of the Si Chip = $1.017 \times 10^{-5} \text{ W/}^\circ\text{C-mm}^2$

Ambient Temperature = 55°C

The back of the GaAs Chip = $0.982 \times 10^{-5} \text{ W/}^\circ\text{C-mm}^2$

The side of the GaAs Chip = $2.596 \times 10^{-5} \text{ W/}^\circ\text{C-mm}^2$

The top of the GaAs Chip = $2.596 \times 10^{-5} \text{ W/}^\circ\text{C-mm}^2$

The back of the Si Chip = $2.142 \times 10^{-5} \text{ W/}^\circ\text{C-mm}^2$

The side of the Si Chip = $2.596 \times 10^{-5} \text{ W/}^\circ\text{C-mm}^2$

The top of the Si Chip = $0.9817 \times 10^{-5} \text{ W/}^\circ\text{C-mm}^2$

Concluding Remarks

- A new configuration of VCSEL assembly using solder-bumped flip chip interconnects is proposed
- A 3-D FE thermal analysis is performed to investigate the effect of solder materials and ambient temperature.
- 80Au-20Sn is a better choice than 63Sn-37Pb solder.
- The change of ambient temperature does not affect the pattern of temperature contours.